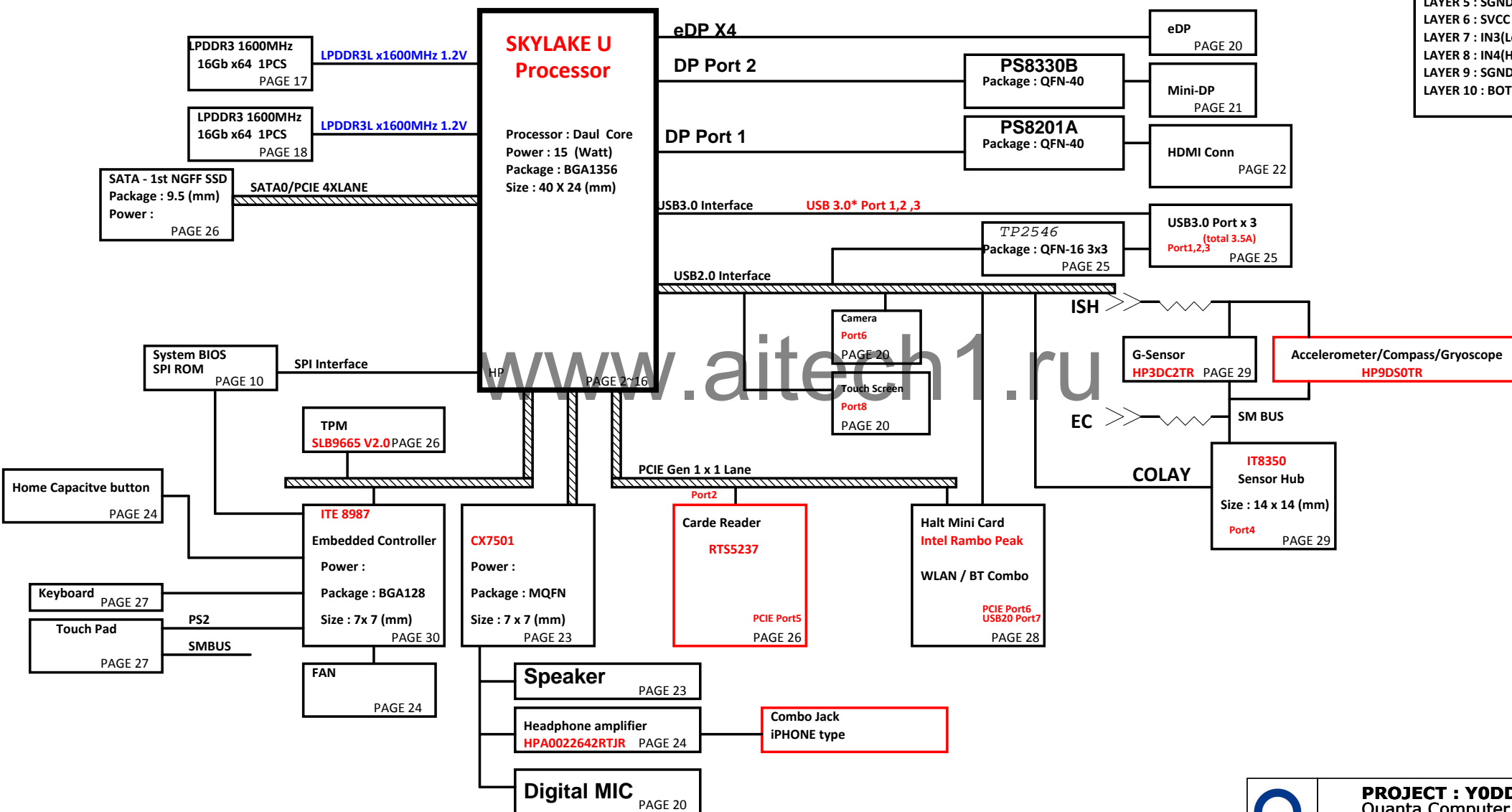
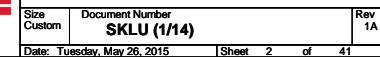


# Pike Intel SKYLAKE ULT Platform Block Diagram

PCB 10L STACK UP

LAYER 1 : TOP  
 LAYER 2 : SGND  
 LAYER 3 : IN1(High)  
 LAYER 4 : IN2(High)  
 LAYER 5 : SGND  
 LAYER 6 : SVCC  
 LAYER 7 : IN3(Low)  
 LAYER 8 : IN4(High)  
 LAYER 9 : SGND  
 LAYER 10 : BOT

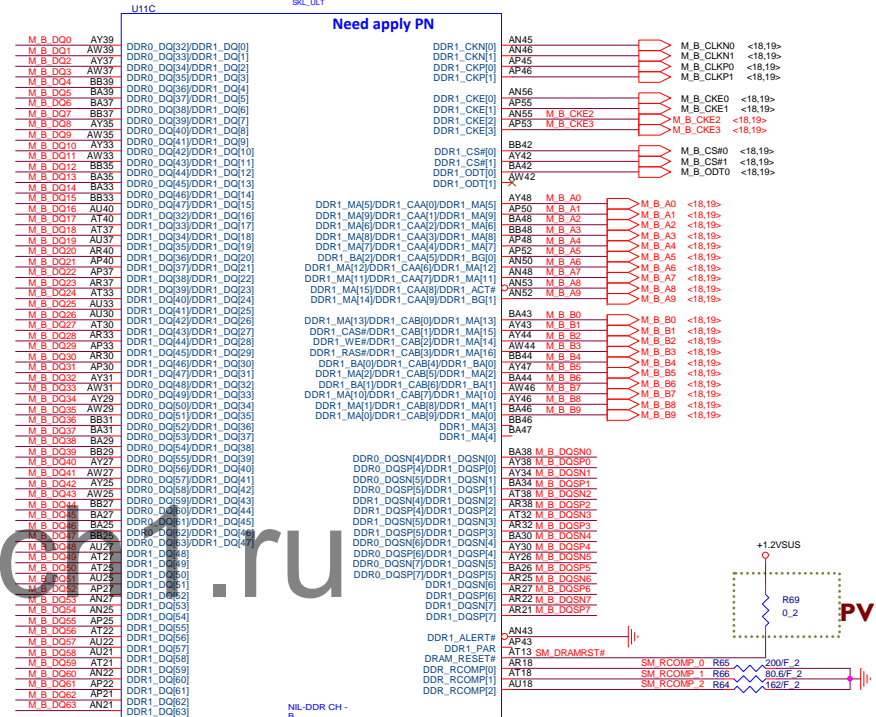
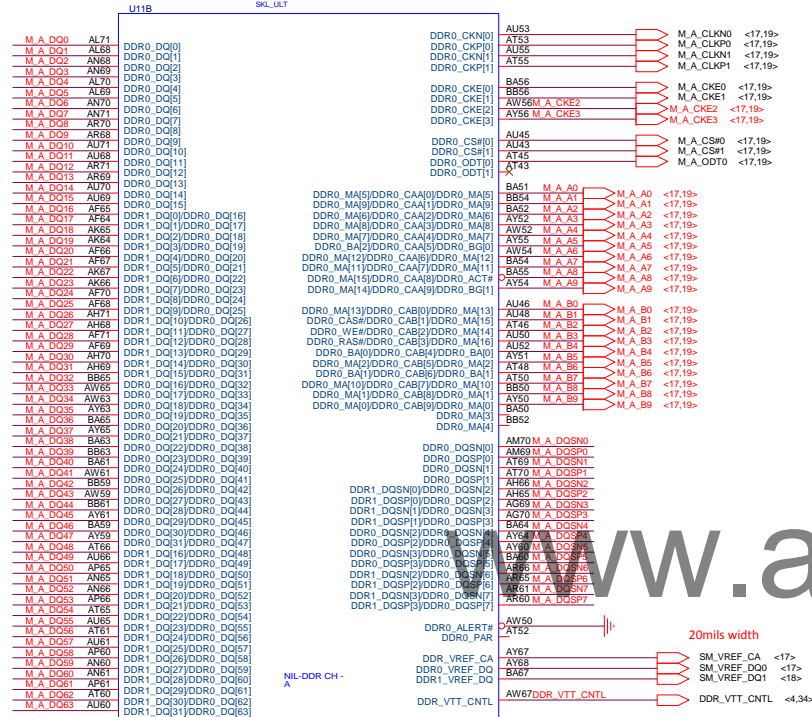




## SkyLake ULT Processor (DDR3L)

Need apply PN

Need apply PN

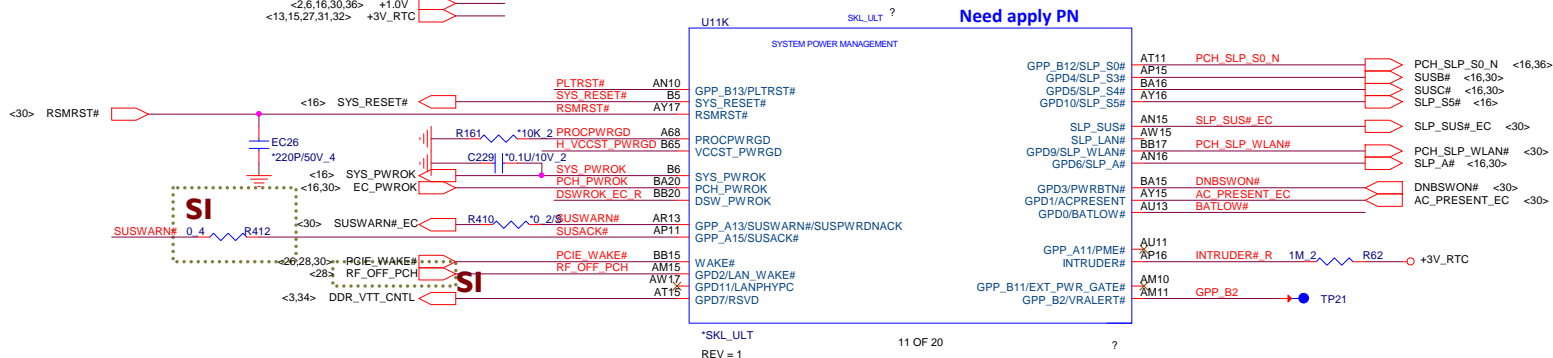
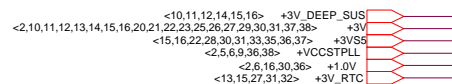


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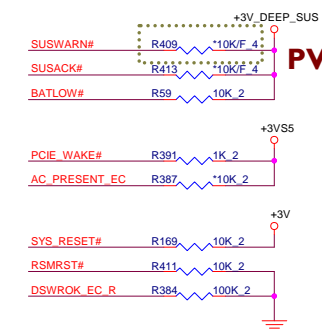


**PROJECT : YODD**  
**Quanta Computer Inc.**

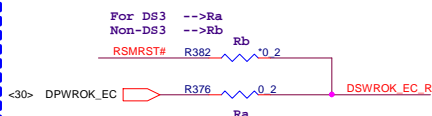
Size Custom Document Number  
 SKL U (2/14)  
 Date: Tuesday, May 26, 2015 Sheet 3 of 41



## PCH Pull-high/low(CLG)

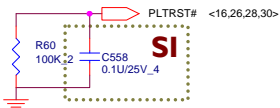


## For DS3 Sequence

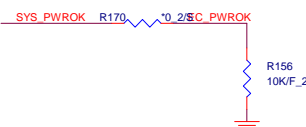
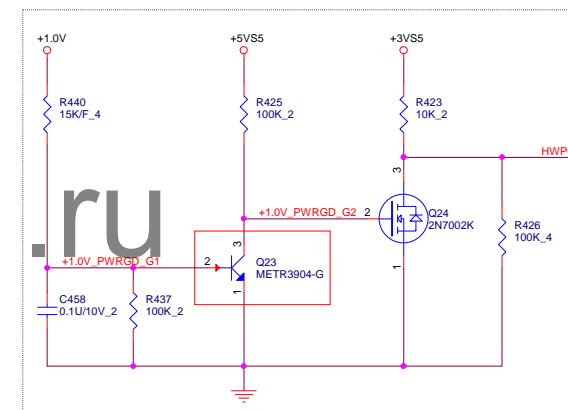
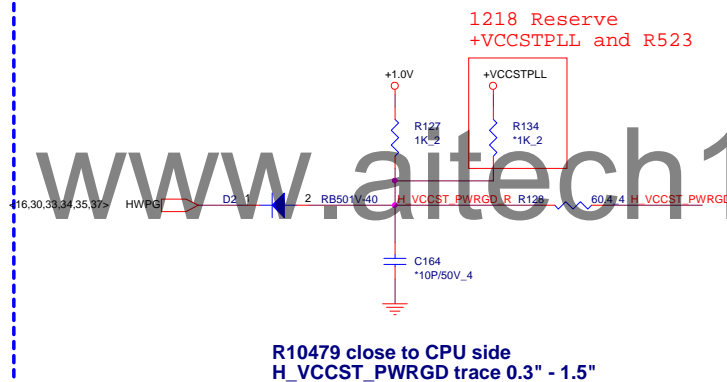


## PLTRST#(CLG)

Check Q2010 Rise/Fall time less than 100ns




## System PWR\_OK(CLG)

1218 Reserve  
+VCCSTPLL and R523

1110 Add Circuit for +1.0V Power Good

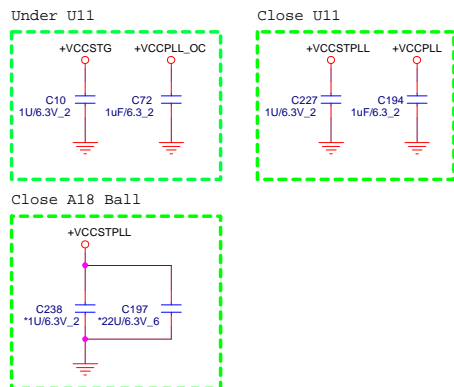
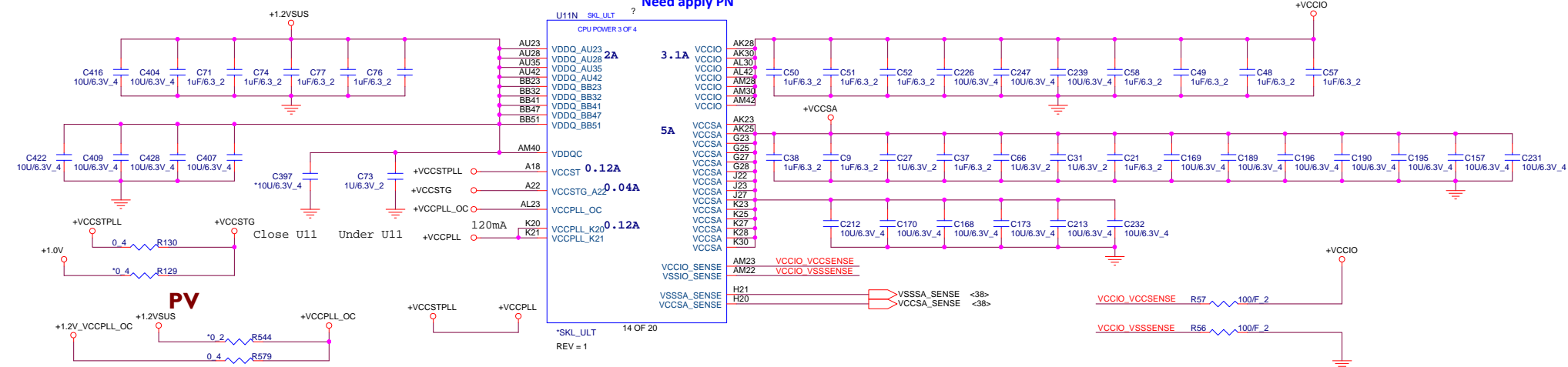
1118 Change Change Q7062 P/N from BA051440000 to  
BA039040020, Del D7002,D7003, R10526, R10527



	<b>PROJECT : YODD</b> Quanta Computer Inc.		
	Size Custom	Document Number <b>SKL U (4/14)</b>	Rev 1A
	Date: Tuesday, May 26, 2015	Sheet 5 of 41	

+VCCSTPLL <2.4,5.9,36,38>  
 +VCCSA <36,39>  
 +1.2VSUS <3,17,18,34,36>  
 +1.0V\_DEEP\_SUS <9,13,15,16,35,36>  
 +1.0V <2.4,16,30,36>  
 +3VPCU <13,15,27,28,30,31,32,33,41>  
 +1.2V\_VCCPLL\_OC <36>

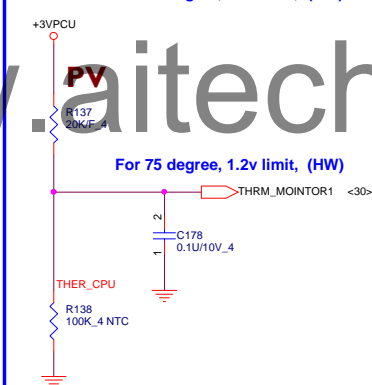
Need apply PN



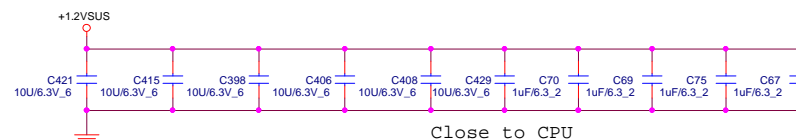
## IO Thrm Protect

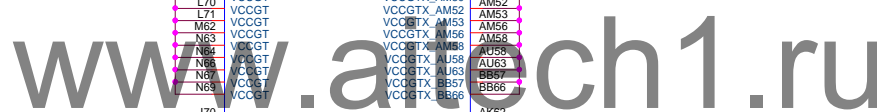
For 65 degree, 1.8v limit, (SW)

For 75 degree, 1.2v limit, (HW)

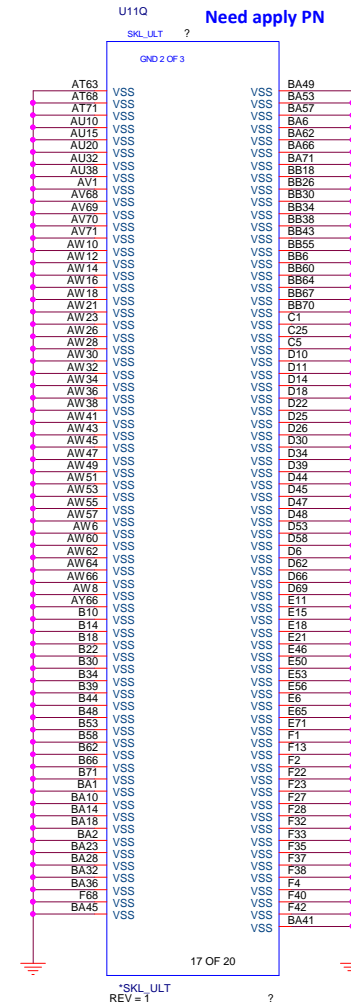
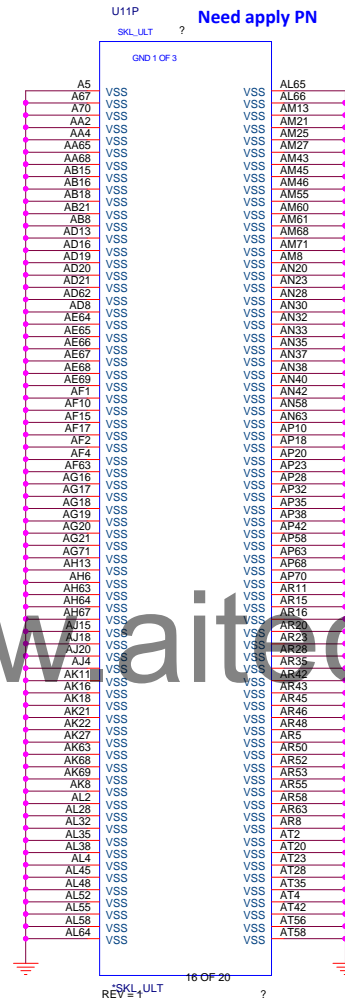
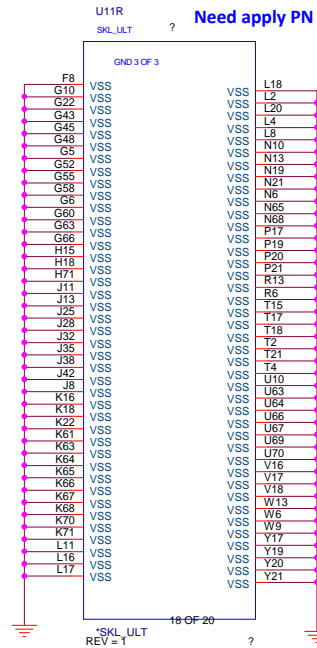


Power Rail	Description	Control
V <sub>CC</sub>	Processor IA Cores Power Rail	SVID
V <sub>CCGT</sub>	Processor Graphics Power Rails	SVID
V <sub>CCGTx</sub>	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V <sub>CCSA</sub>	System Agent Power Rail	SVID/Fixed (SKU dependent)
V <sub>CCIO</sub>	IO Power Rail	Fixed
V <sub>CCST</sub>	Sustain Power Rail	Fixed
V <sub>CCPLL</sub>	Processor PLLs power rail	Fixed
V <sub>DDQ</sub>	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V <sub>CCOPC</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCOPC_1P8</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCePIO</sub>	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

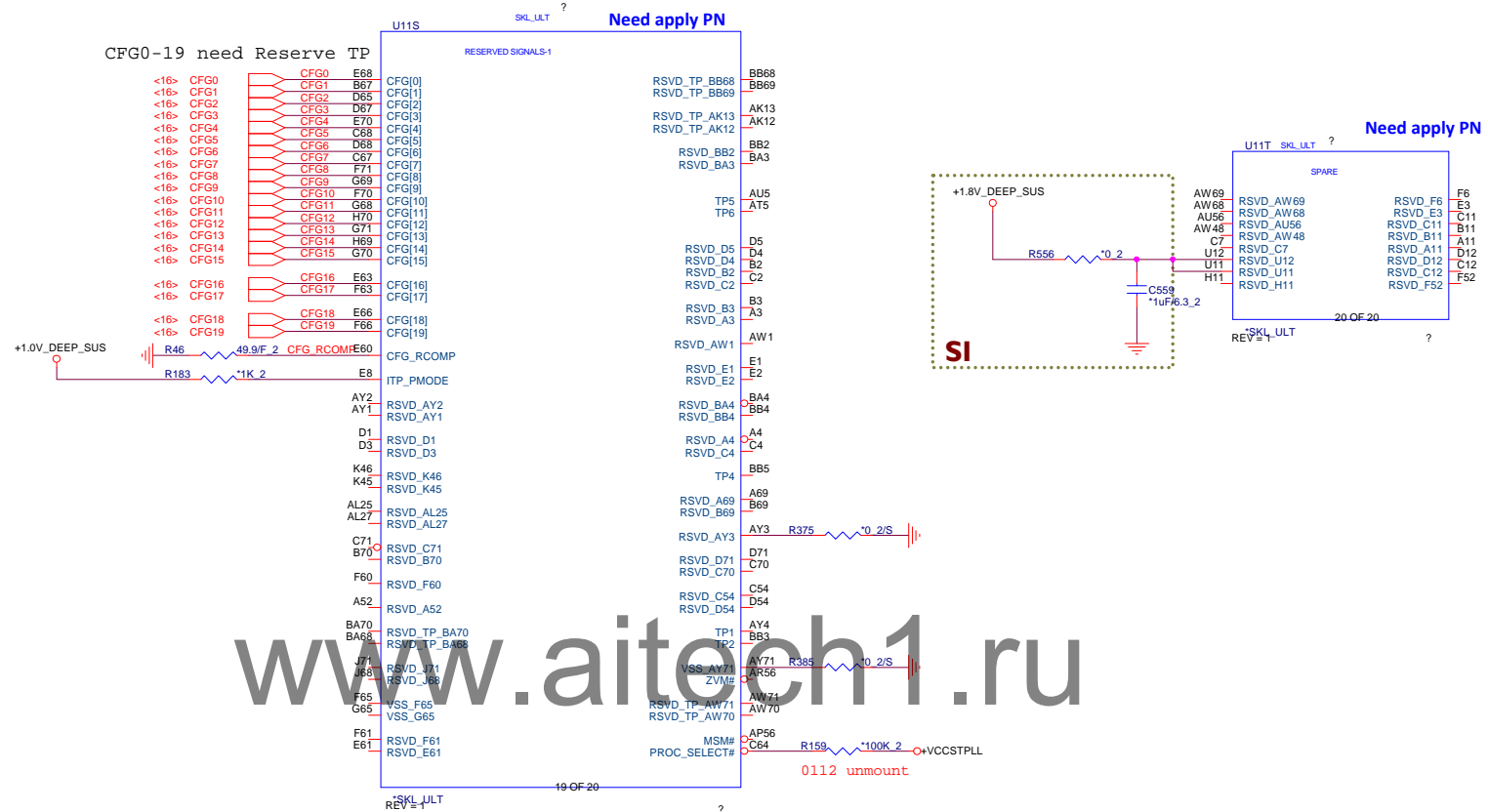




\*SKL\_ULT 13 OF 20  
REV = 1







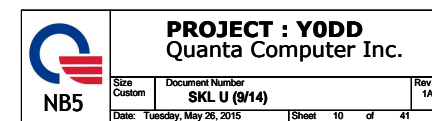
### Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physical Debug Enable) DFX_Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R143 *1K 2
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R42 *1K 2

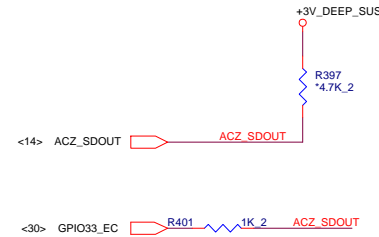
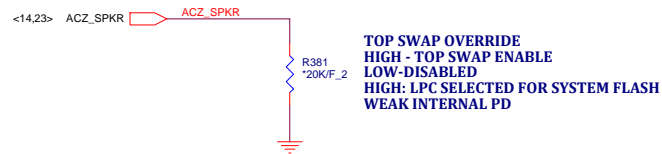


### 4M SPI ROM Socket



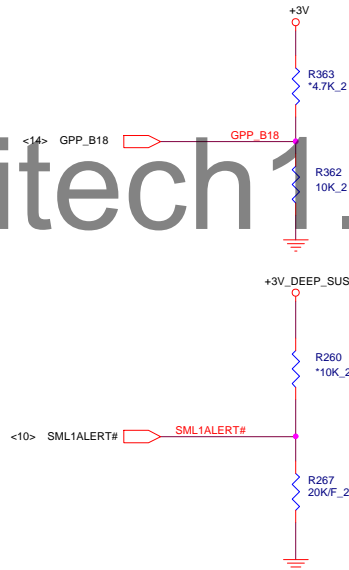
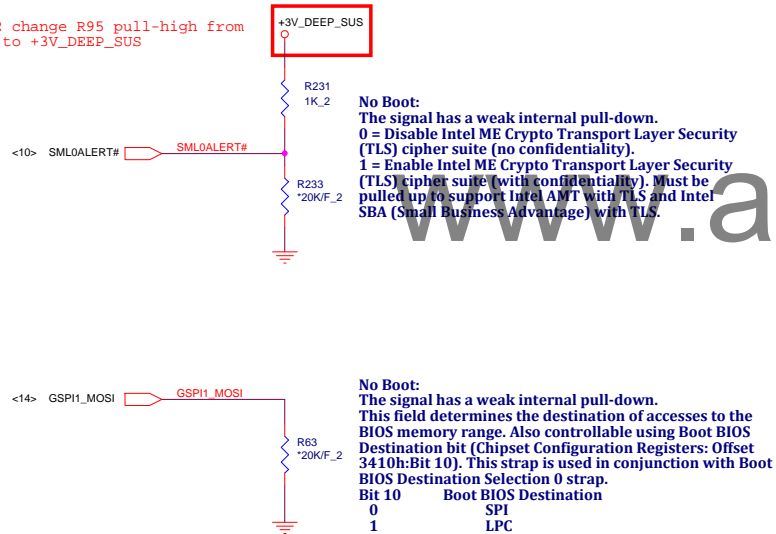
# Functional Strap Definitions

**DESIGN NOTE:**  
WEAK PULL UP RESISTOR PRESENT ON THIS NET



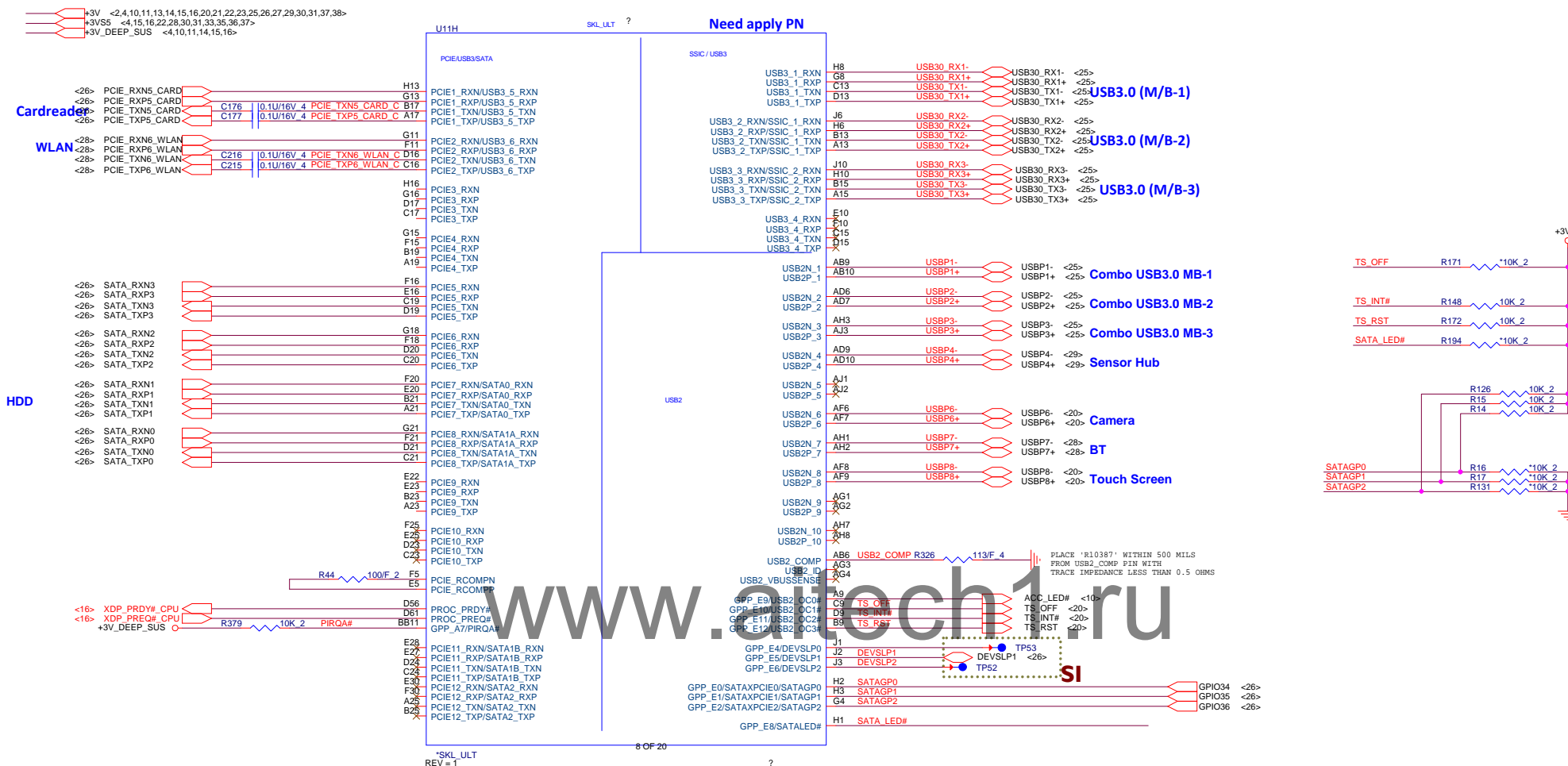
**No Boot:**  
The signal has a weak internal pull-down.  
0 = Enable security measures defined in the Flash Descriptor.  
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.

1212 change R95 pull-high from +3V to +3V\_DEEP\_SUS

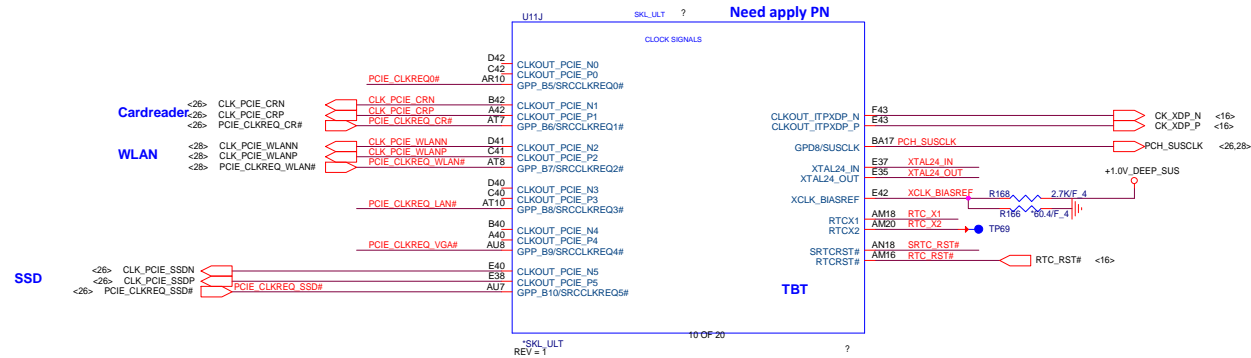


**No Boot:**  
The signal has a weak internal pull-down.  
0 = Disable No Reboot mode.  
1 = Enable No Reboot mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

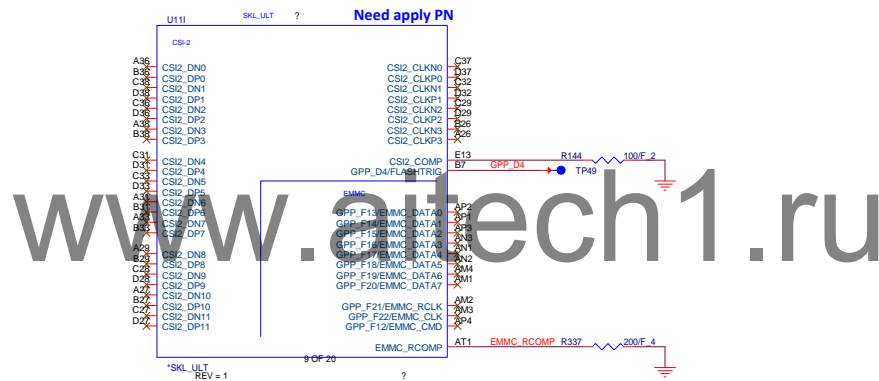
**No Boot:**  
The signal has a weak internal pull-down.  
0 = LPC is selected for EC.  
1 = eSPI is selected for EC.



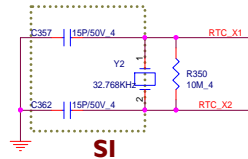

 +1.8V\_DEEP\_SUS <9,15,35,37>  
 +3V <2,4,10,11,12,14,15,16,20,21,22,23,25,26,27,29,30,31,37,38>



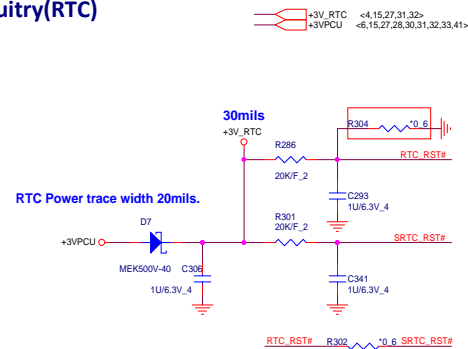
**CLK\_REQ/Strap Pin(CLG)**



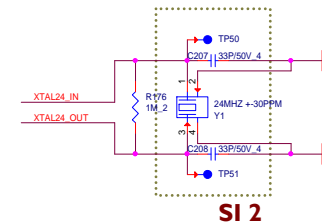
**RTC Clock 32.768KHz**



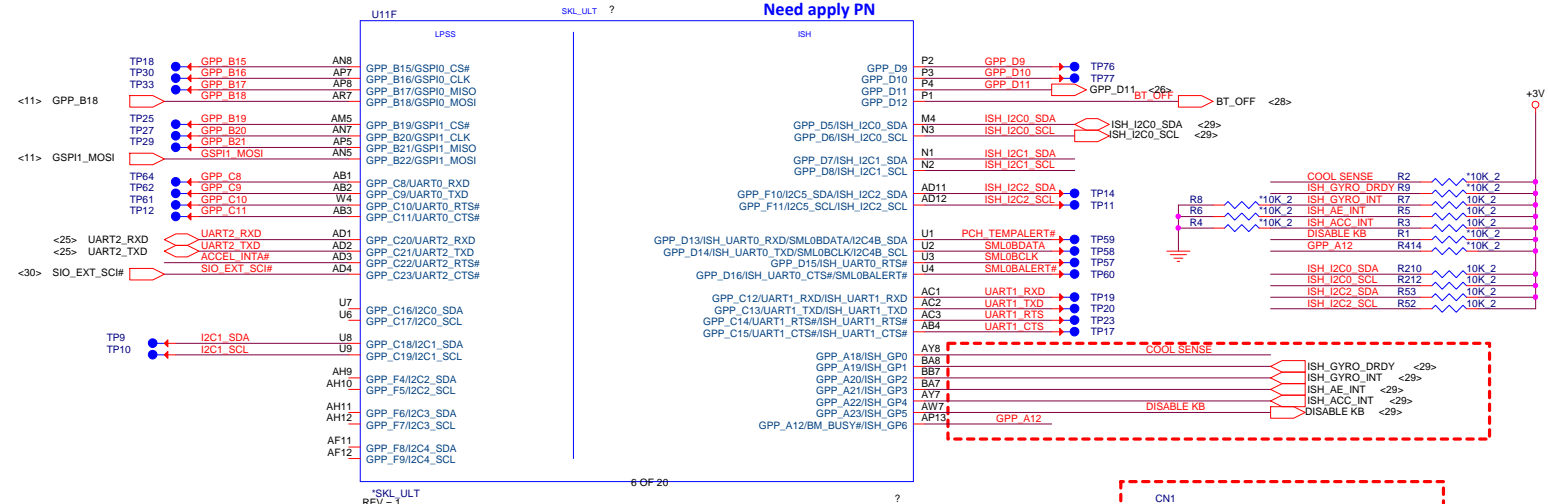
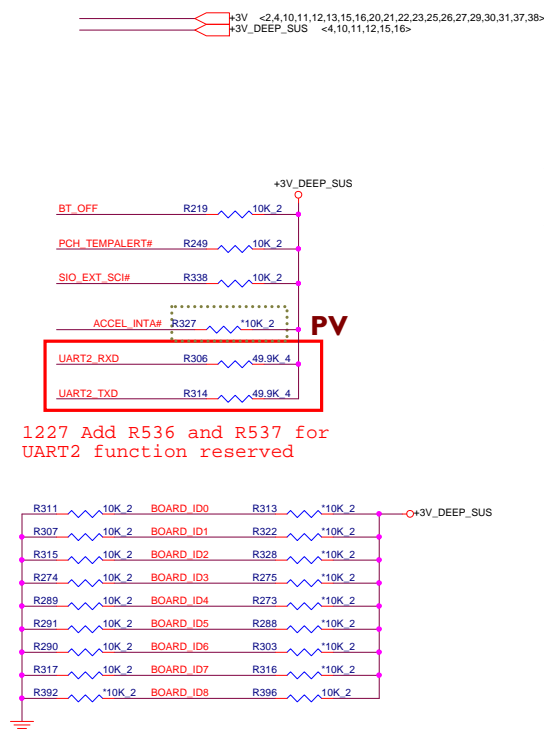
## RTC Circuitry(RTC)



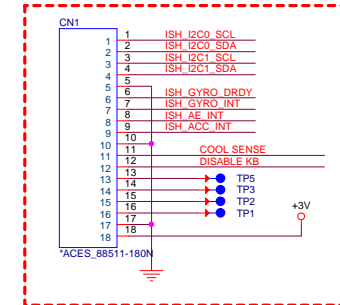
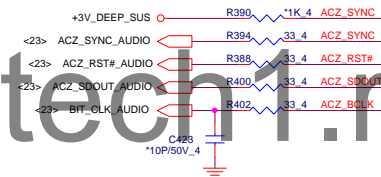
## External Crystal



## Skylake (GPIO)

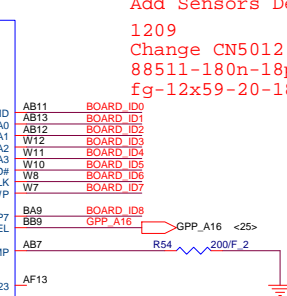
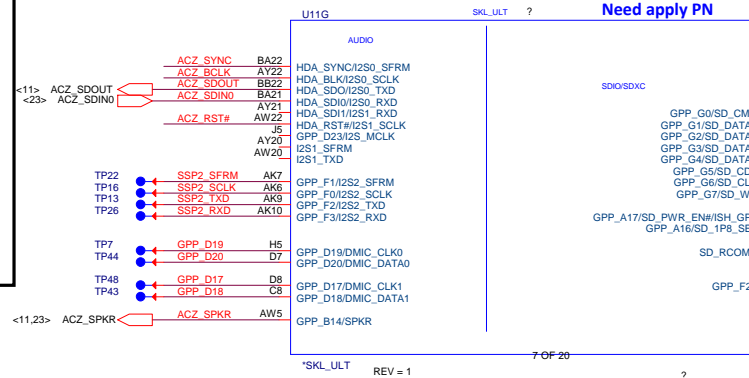


## HDA Bus(CLG)



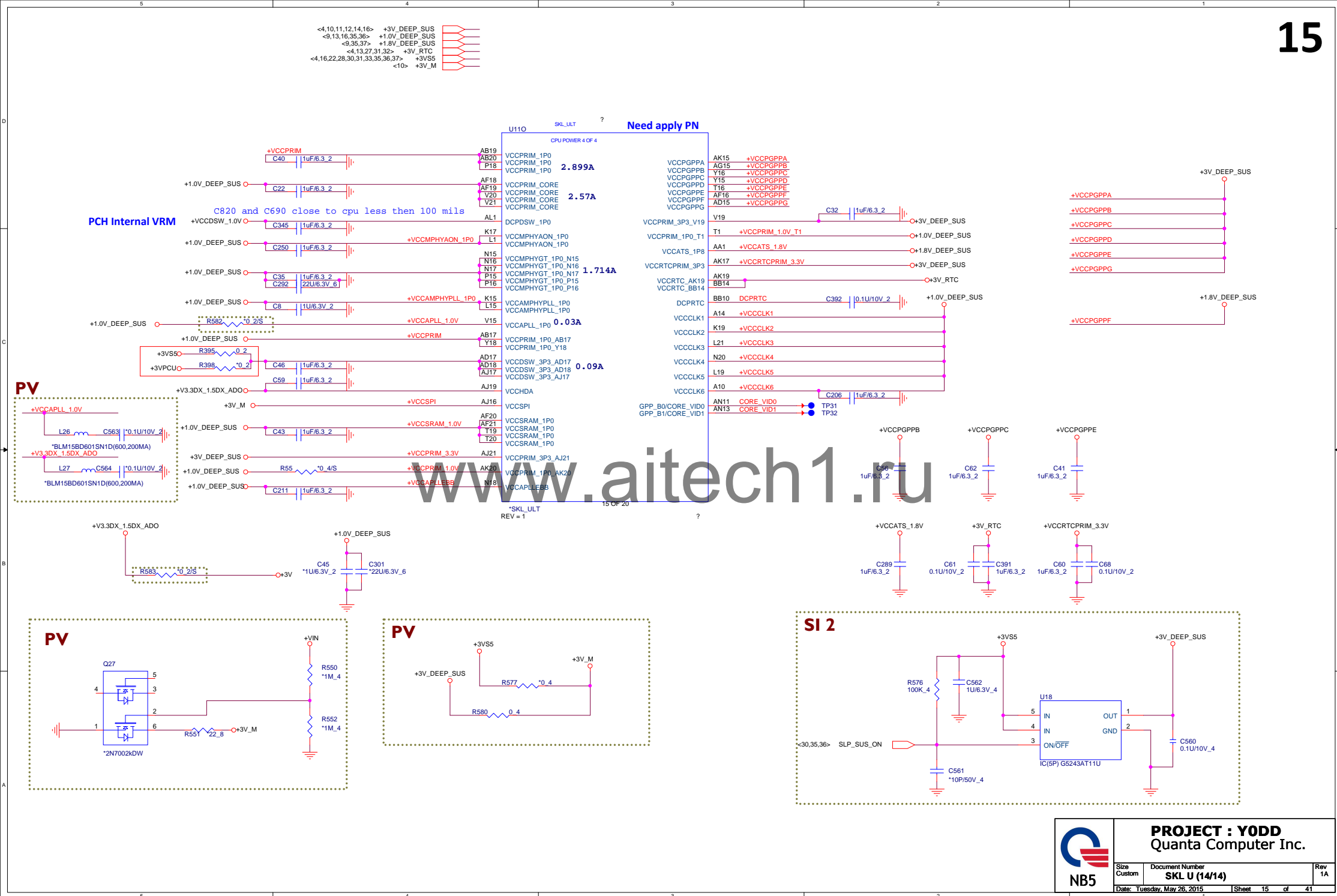
1207 Add Sensors Debug CONN  
1209 Change CN5012 footprint from 88511-180m-18p-1 to fg-12x59-20-18p

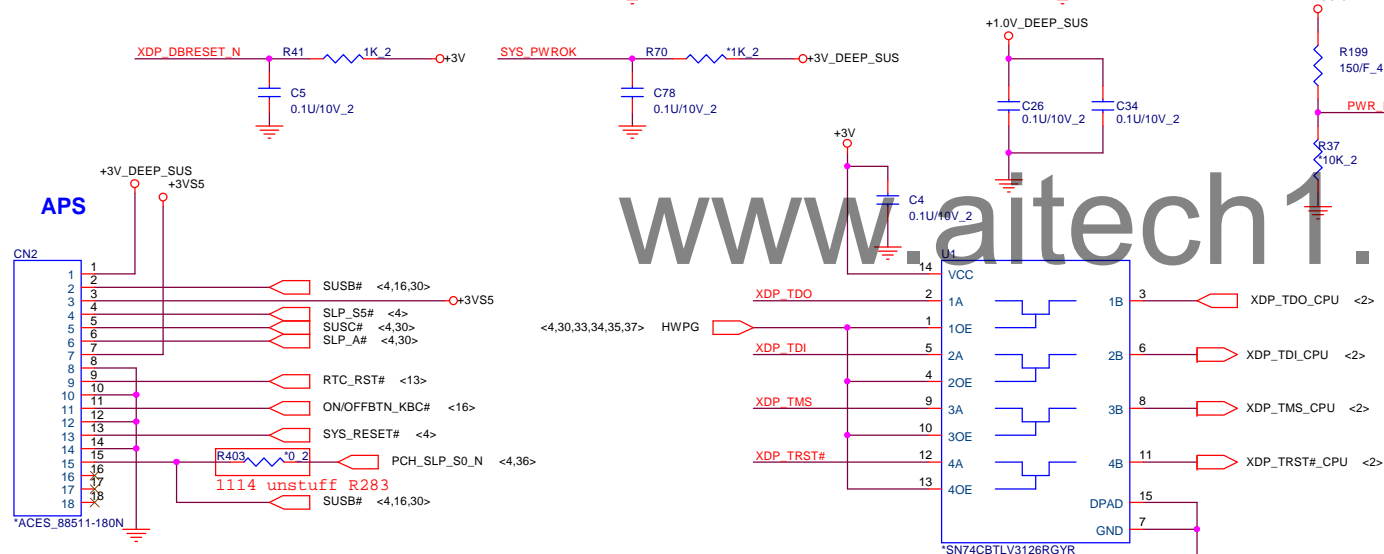
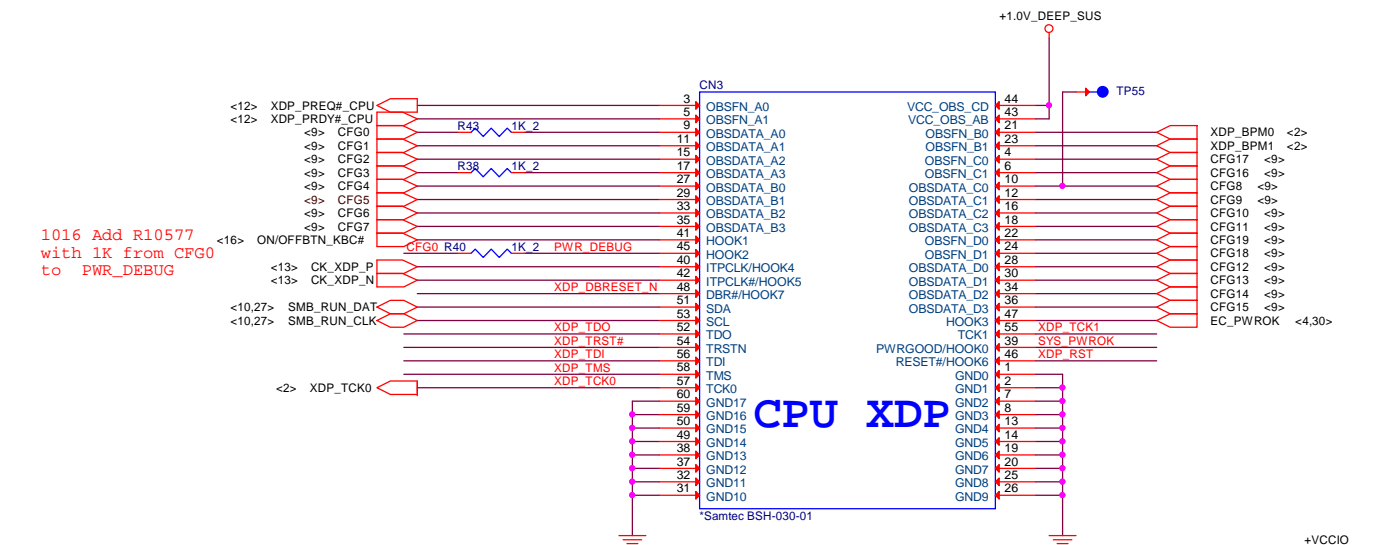
Model	BOARD_ID6	BOARD_ID7	Board ID [6:4]	BOARD_ID[3:1]	BOARD_ID0
Y0DD	0:VPRO 1:non-VPRO	0:2+2 CPU 1:2+3E CPU	Reserve (Default = 00)	000:H9CCNNNBKTMLBR-NTD Hynix 4G 1600 001:EDFA164A2MA-GD-F ELPIDA 4G 1600 010:K3QF2F20EM-AGCF Samsung 4G 1866 011: Hynix 4G 1866 100:ELPIDA 4G 1866  000:H9CCNNNCPTMLBR-NTD Hynix 8G 1600 001:EDFB164A1MA-GD-F Micron 8G 1600 010: Samsung 8G 1866 011:H9CCNNCPTMLBR-NUD Hynix 8G 1866 100: ELPIDA 8G 1866	0:4G 1:8G



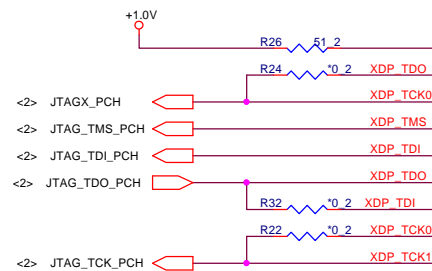
**PROJECT : Y0DD**  
Quanta Computer Inc.

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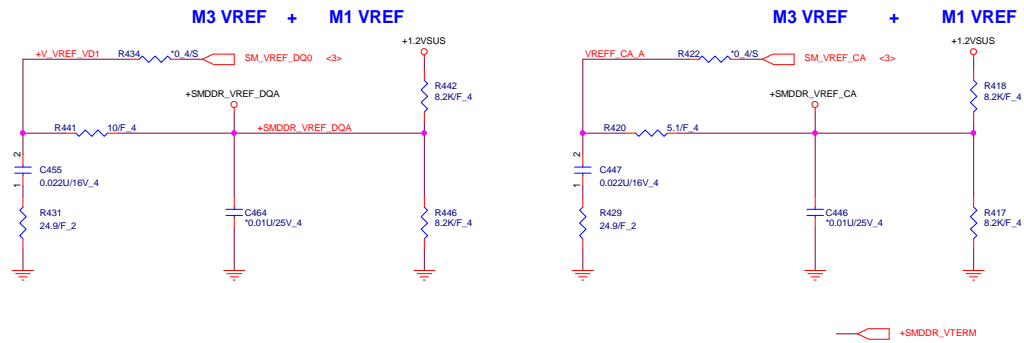
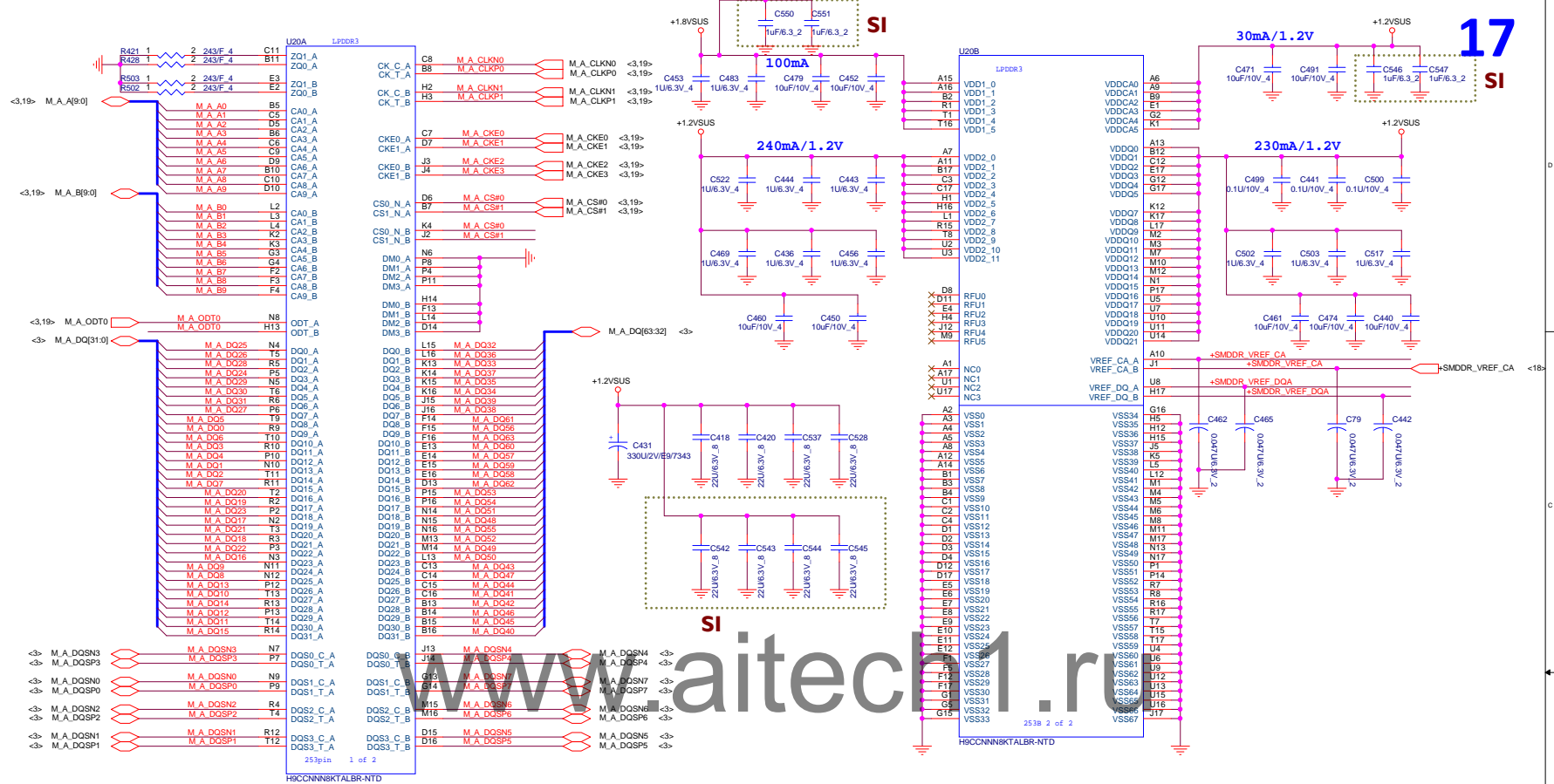
1217  
Change CN5002 footprint from  
88511-180n-18p-1 to  
fg-12x59-20-18p

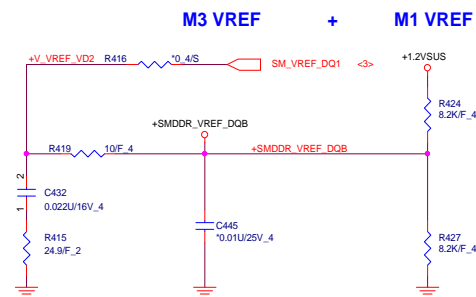


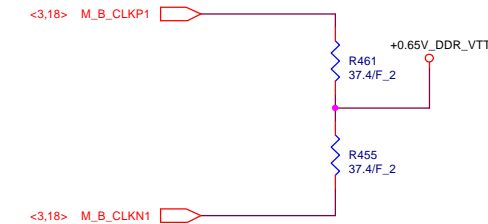
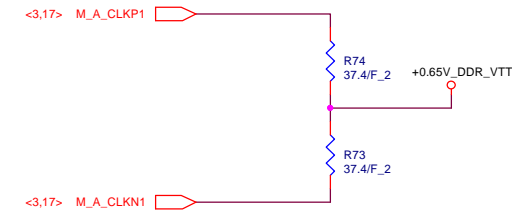
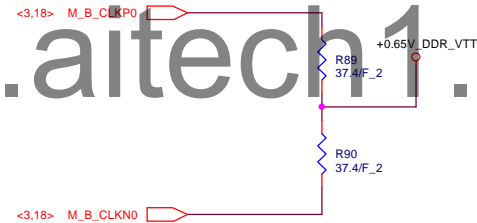
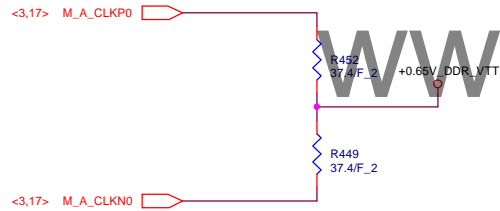
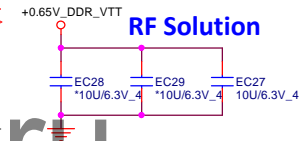
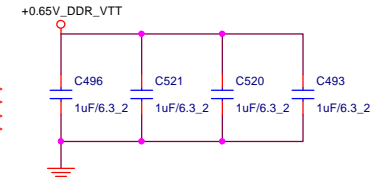
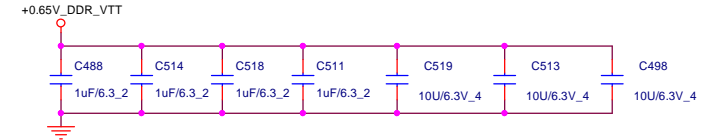
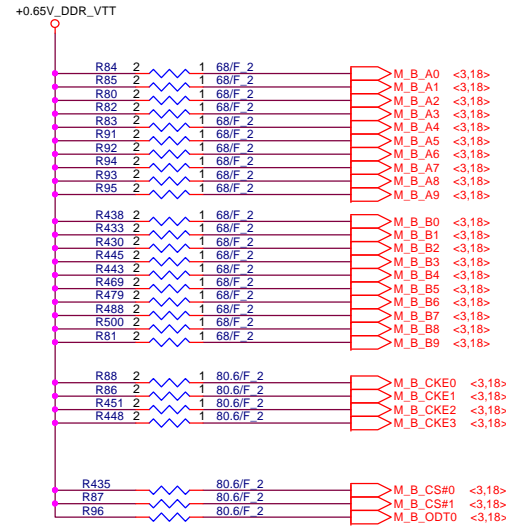
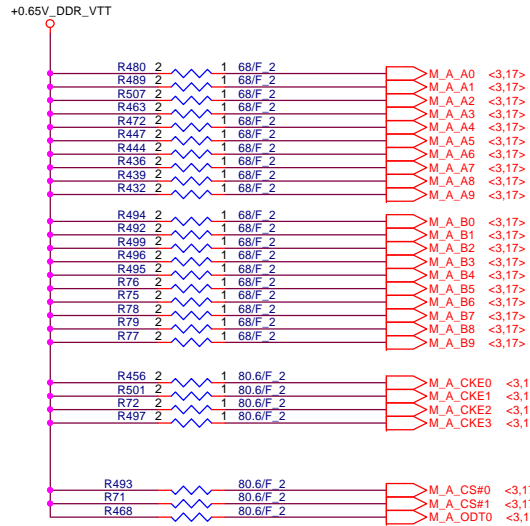
**PROJECT : Y0DD**  
Quanta Computer Inc.

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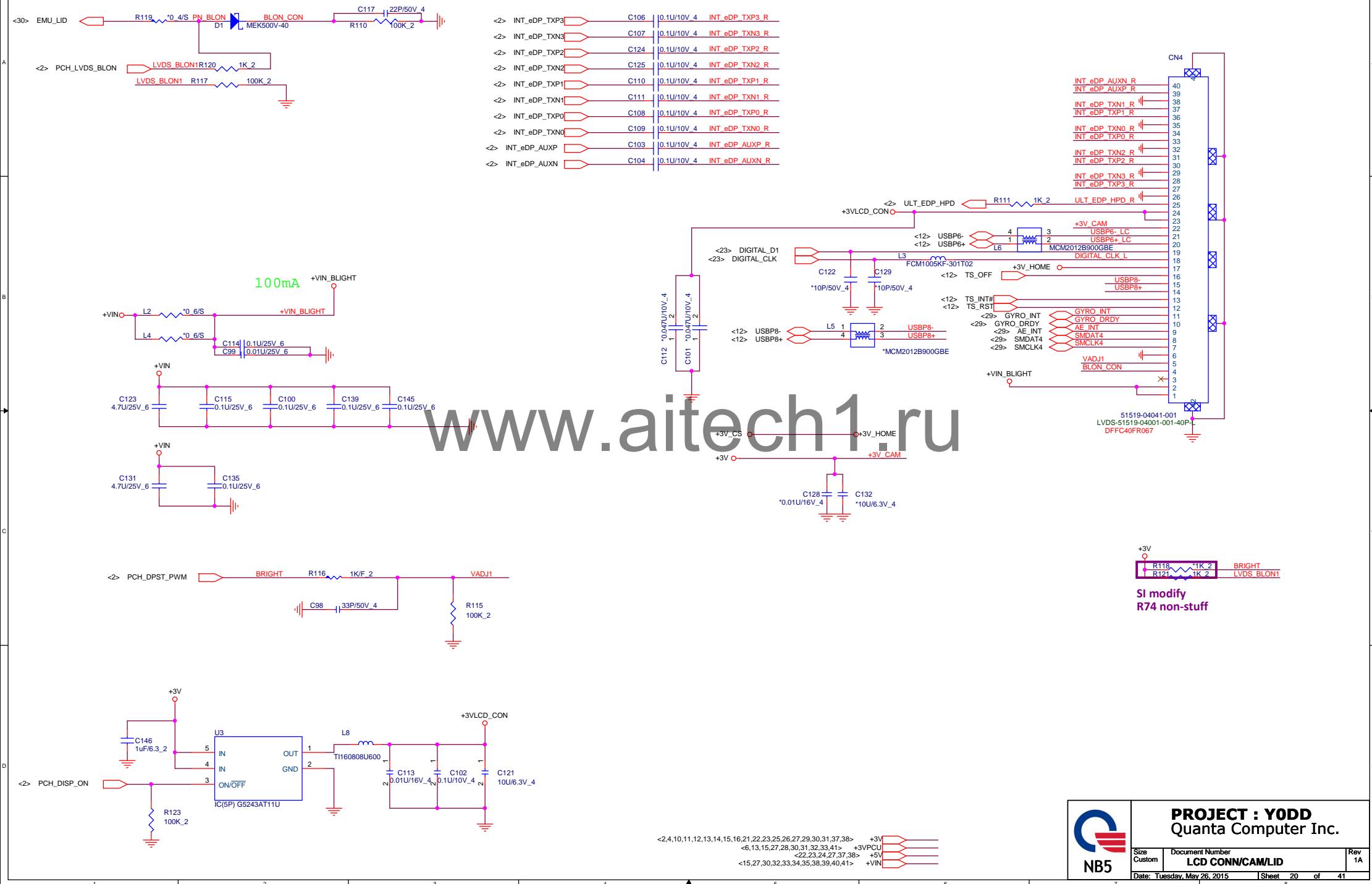


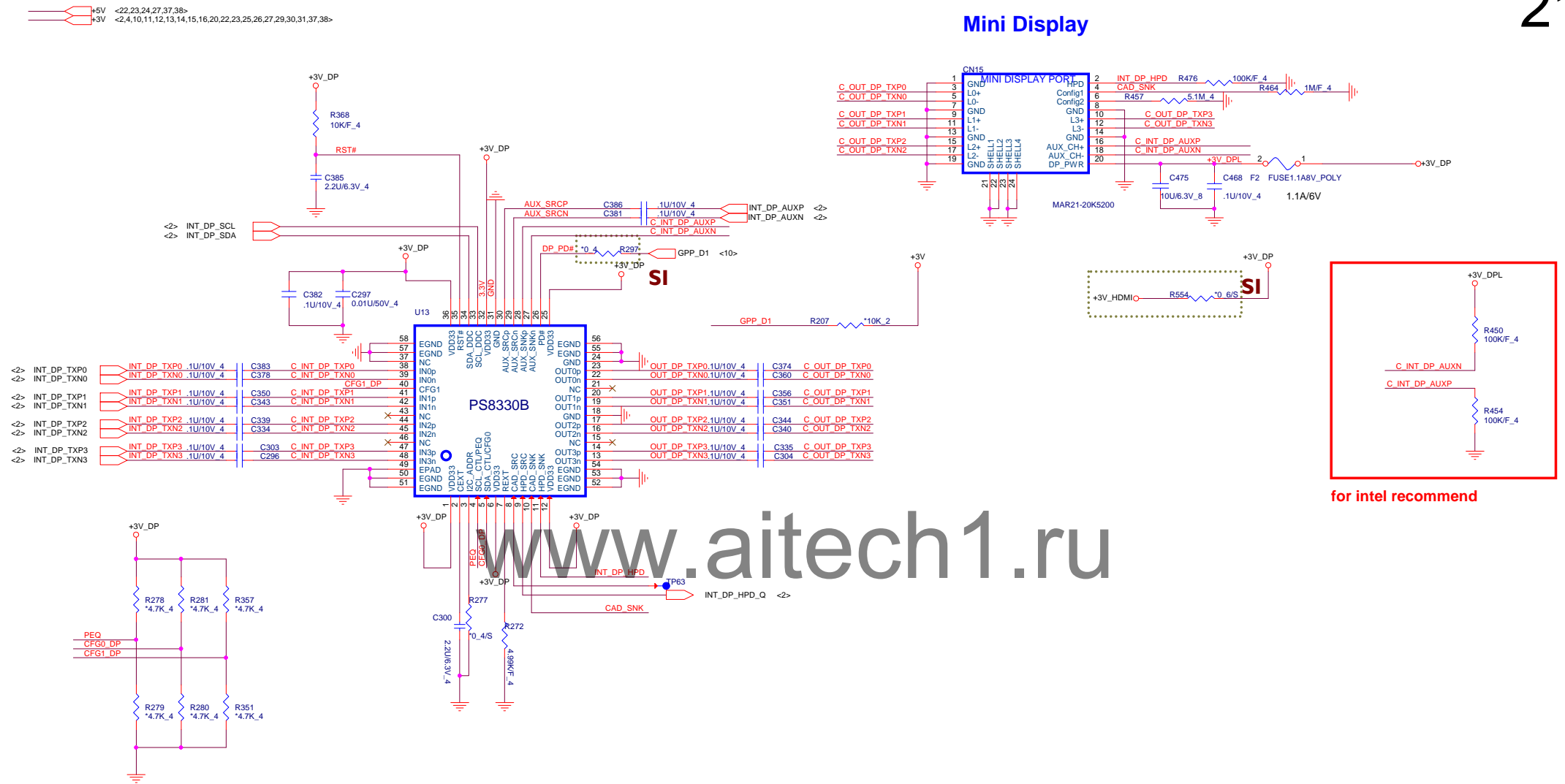


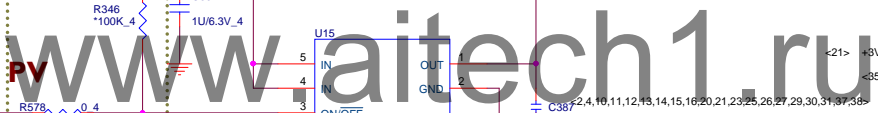
## LID Switch

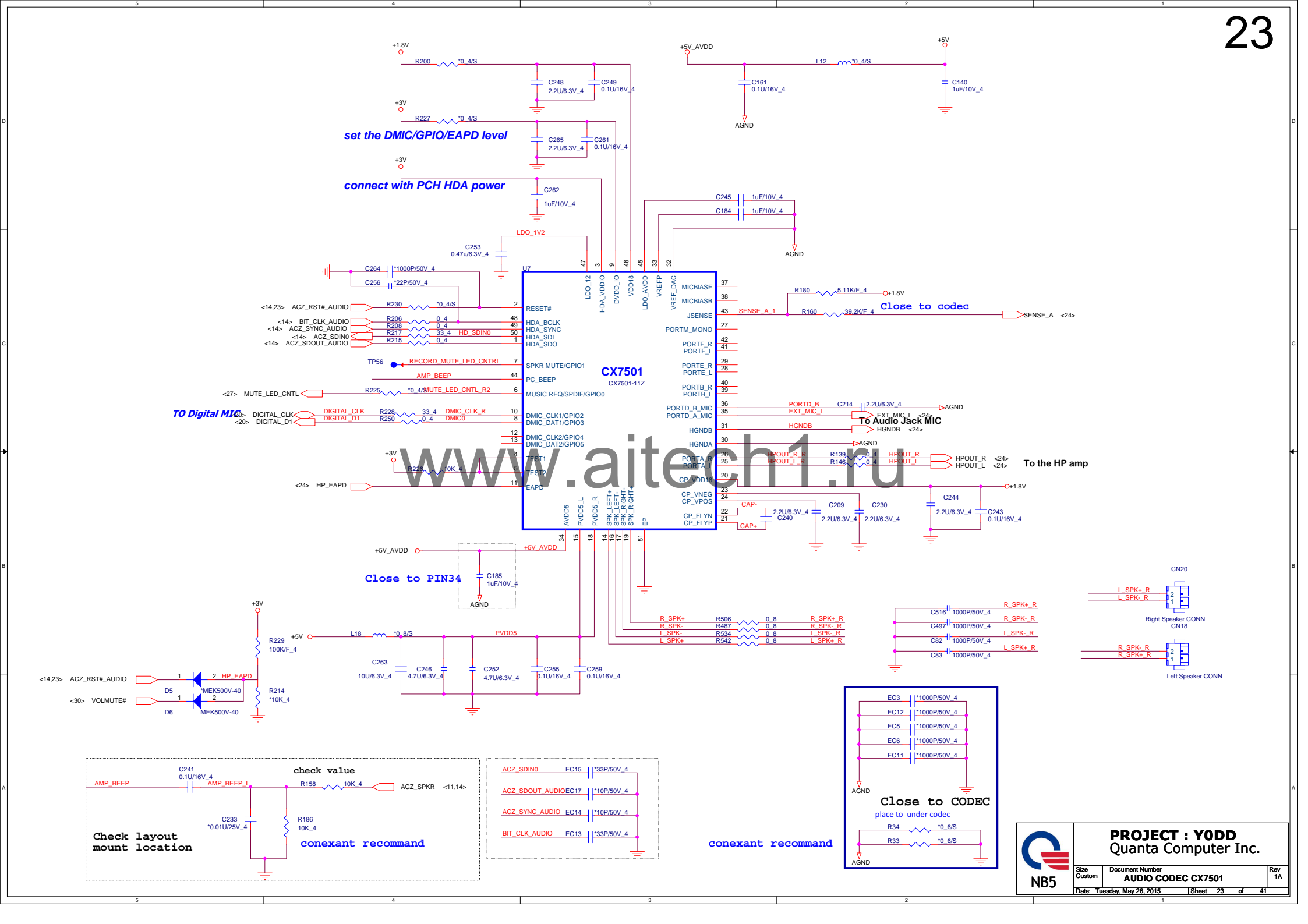
**LVDS Conn.**

20

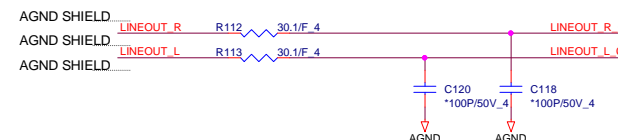
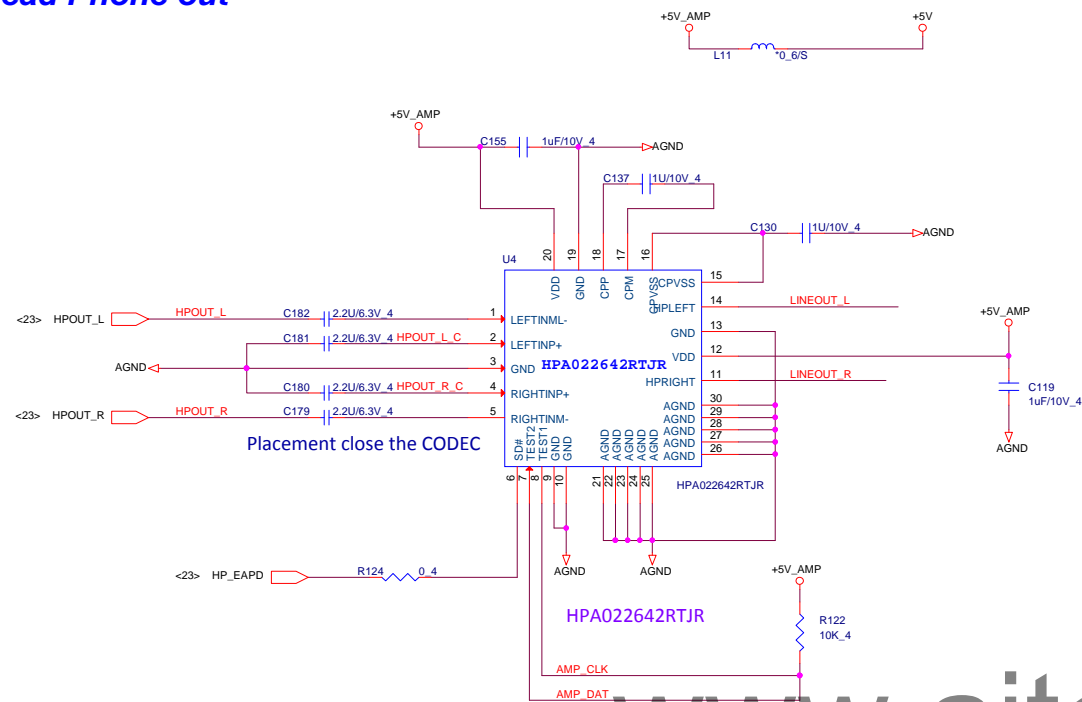








## Head Phone out

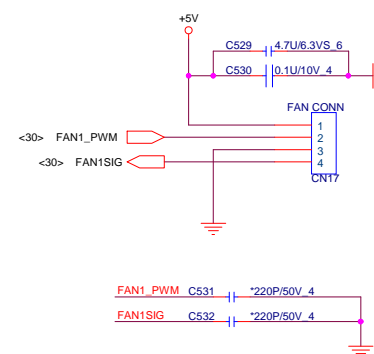
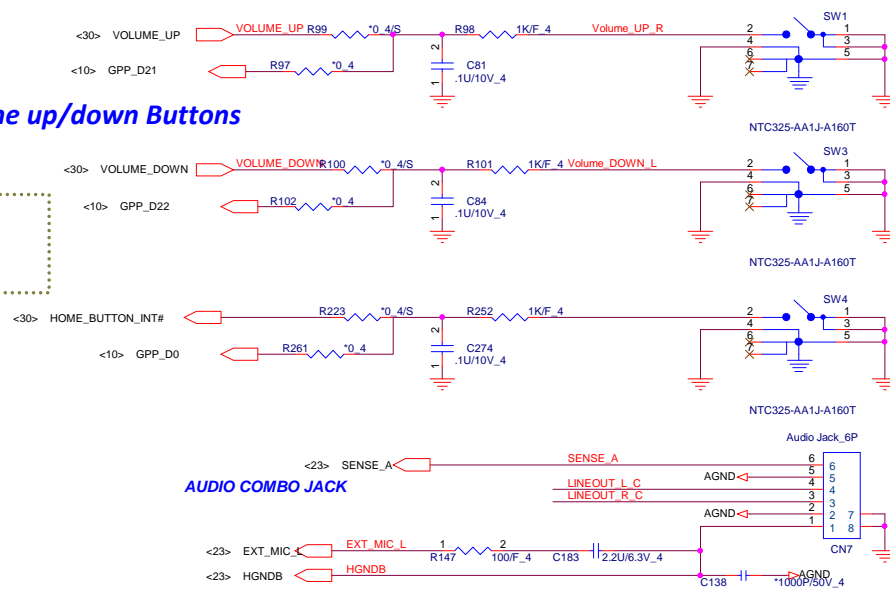


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## Audio combo JACK &amp; Volume up/down Button

## FAN

## Volume up/down Buttons



<2,4,10,11,12,13,14,15,16,20,21,22,23,25,26,27,29,30,31,37,38> +3V  
 <22,23,27,37,38> +5V  
 <4,25,33,34,35,36,37> +5VSS

NB5	<b>PROJECT : YODD</b> Quanta Computer Inc.		
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2



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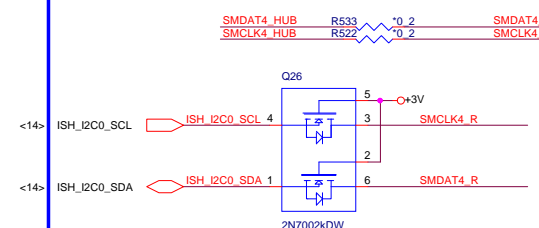
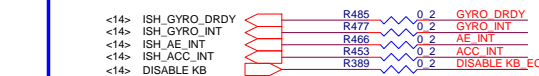
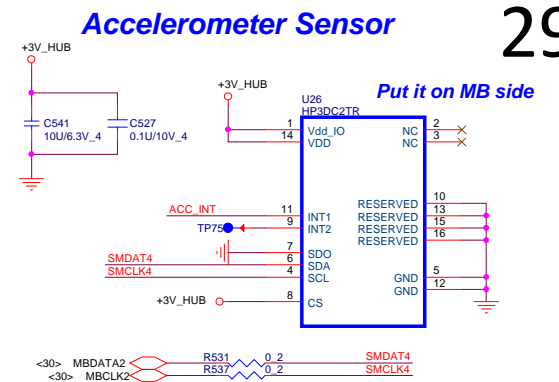


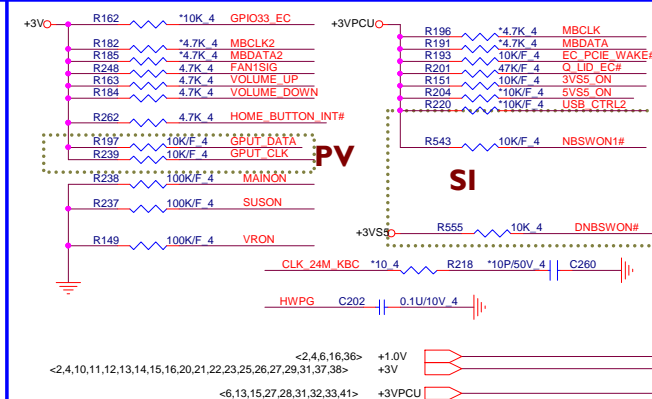
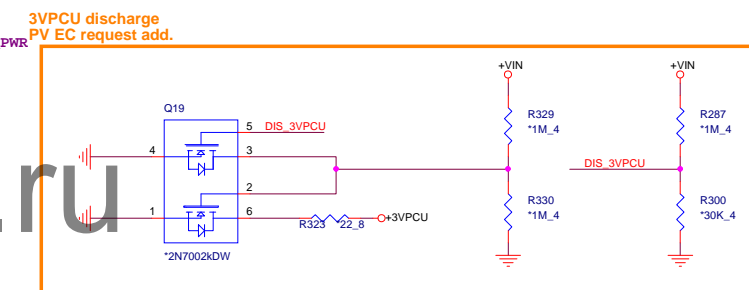
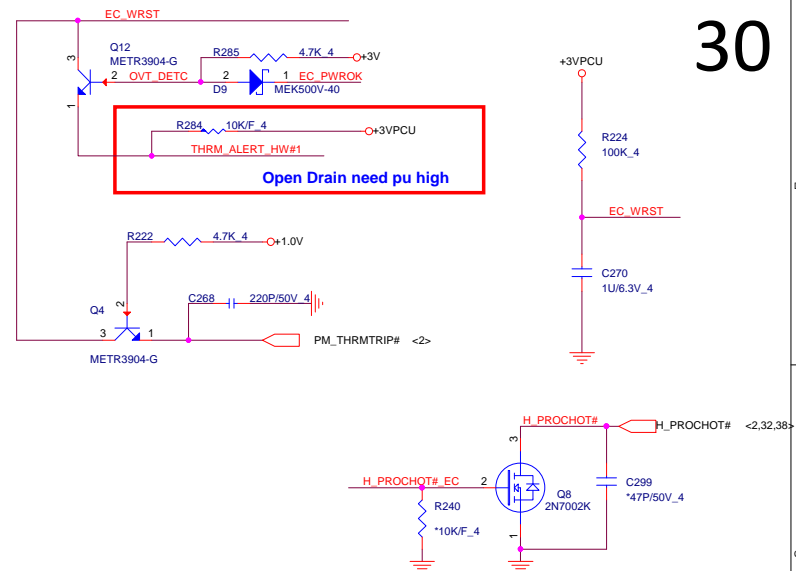
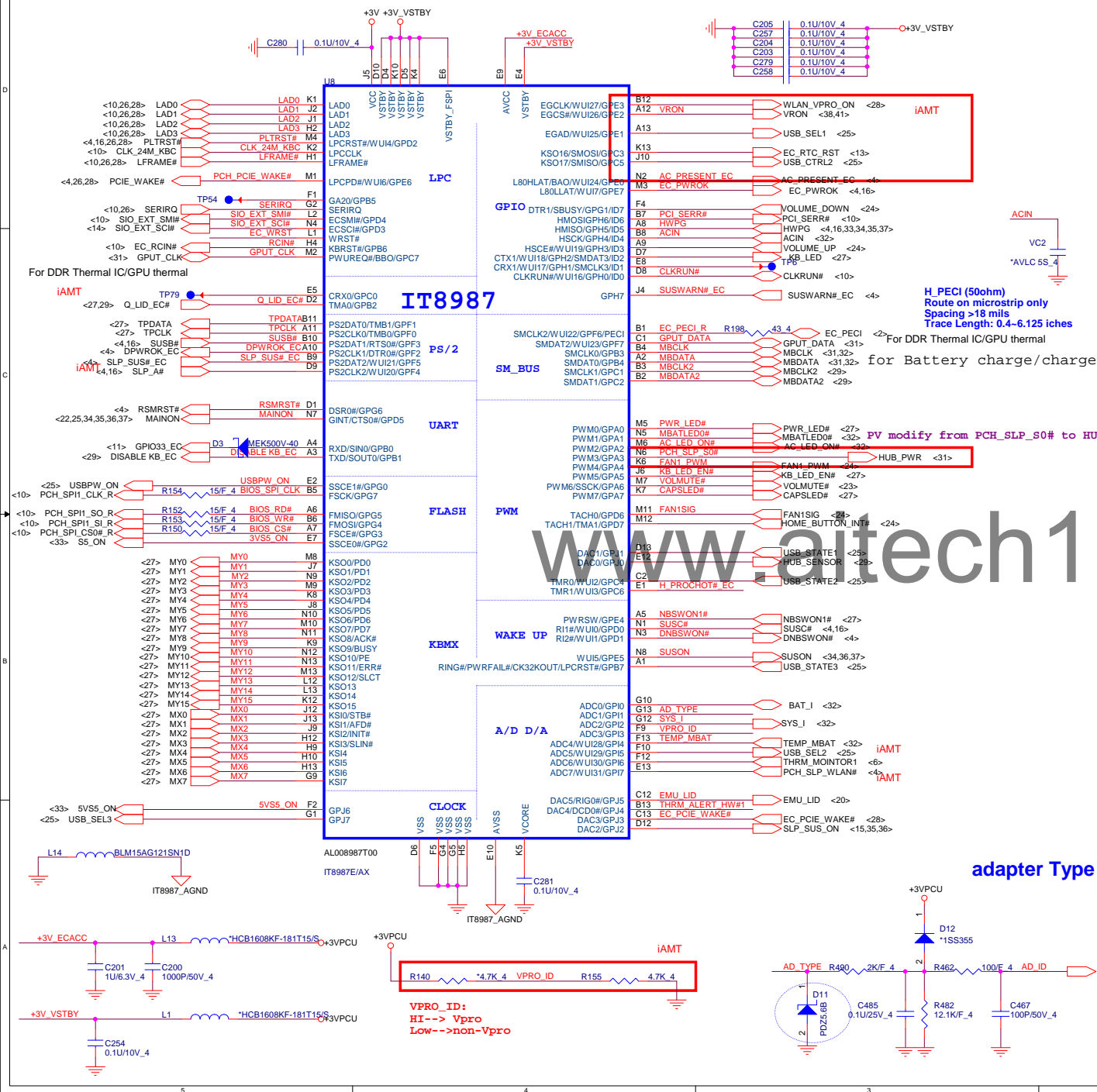
The diagram illustrates the 16-channel readout system for the ATLAS LHCb upgrade. It shows 16 channels, each consisting of a detector (SPAD or H-C) connected to a readout circuit. The channels are labeled H1 through H16 and SPAD1 through SPAD13. The readout circuit includes a preamplifier, a discriminator, and a counter. The channels are arranged in a grid-like structure.

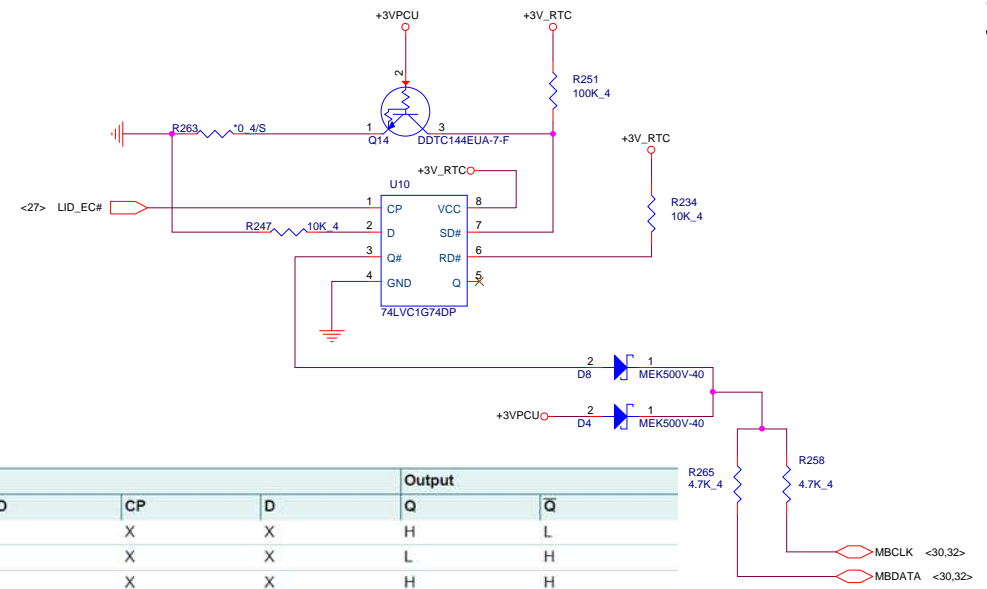
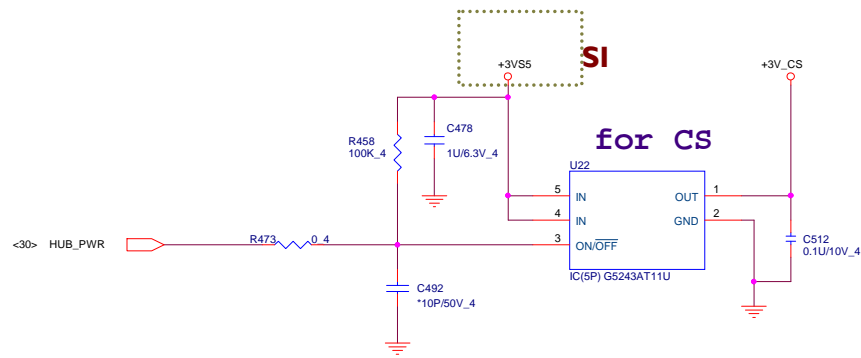
The channels are labeled as follows:

- H14:  $^3\text{H-TC315BC213X217D181P2}$
- H8:  $^3\text{H-C315D142P2}$
- H1:  $^3\text{H-TC315BC236D106P2}^3\text{H-Y0DX-1}$
- H4:  $^3\text{H-C315D91P2}$
- H3:  $^3\text{H-PIKE-4}$
- H2:  $^3\text{H-C157D118P2}$
- H5:  $^3\text{H-TC315IC182BC142D142P2}$
- H6:  $^3\text{H-TC315IC182BC142D142P2}$
- H10:  $^3\text{H-TC315IC182BC142D142P2}$
- H9:  $^3\text{H-TC315IC182BC142D142P2}$
- H16:  $^3\text{H-TC236BC315D142P2}$
- H13:  $^3\text{H-Y0DX-2}$
- SPAD13:  $^3\text{SPAD-C236}$
- SPAD7:  $^3\text{SPAD-pike-2}$
- SPAD5:  $^3\text{SPAD-C236}$
- SPAD3:  $^3\text{SPAD-C236}$
- SPAD1:  $^3\text{SPAD-C236}$
- SPAD2:  $^3\text{SPAD-C236}$
- SPAD4:  $^3\text{SPAD-C236}$
- SPAD8:  $^3\text{SPAD-C236}$
- SPAD9:  $^3\text{SPAD-pike-3}$
- SPAD11:  $^3\text{SPAD-C236}$
- SPAD6:  $^3\text{SPAD-pike-1}$
- H15:  $^3\text{H-C315D161P2}$
- H7:  $^3\text{H-PIKE-2}$
- H11:  $^3\text{H-PIKE-1}$

Figure 1 displays 12 schematic diagrams of RFPADs (Resistor-Fused Power Addressable Diodes) labeled PAD1 through PAD12. Each diagram shows a circuit with a 100 ohm resistor, a 100 nF capacitor, and a 100 pF capacitor, connected to a 5V source and ground. The diagrams are arranged in a grid-like fashion, with PAD1 to PAD4 in the top row, PAD5 to PAD8 in the middle row, and PAD9 to PAD12 in the bottom row. Each diagram shows a different configuration of the components, with some having the capacitor connected to the 5V source and others to ground.







Input				Output	
SD	RD	CP	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

[1] H = HIGH voltage level;  
L = LOW voltage level;  
X = don't care.

Input				Output	
SD	RD	CP	D	Q <sub>n+1</sub>	Q̄ <sub>n+1</sub>
H	H	↑	L	L	H
H	H	↑	H	H	L

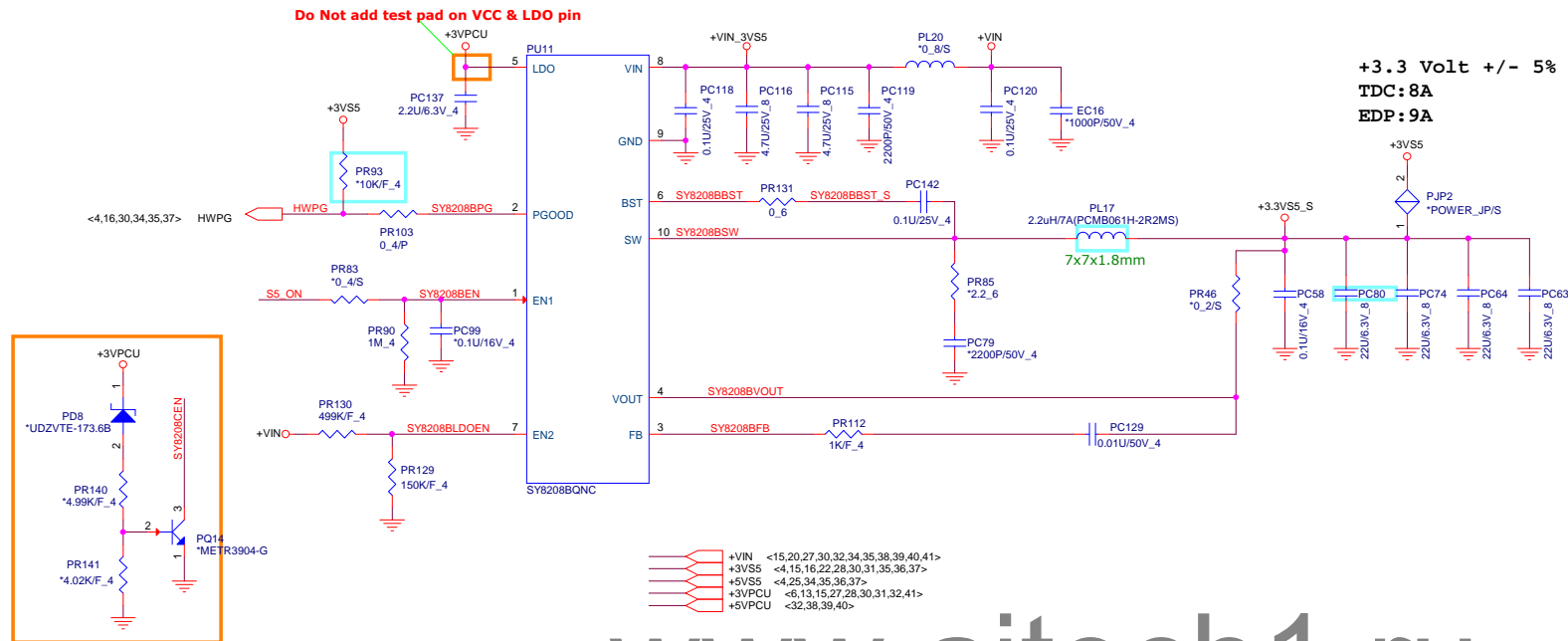
[1] H = HIGH voltage level;  
L = LOW voltage level;  
↑ = LOW-to-HIGH CP transition;  
Q<sub>n+1</sub> = state after the next LOW-to-HIGH CP transition.

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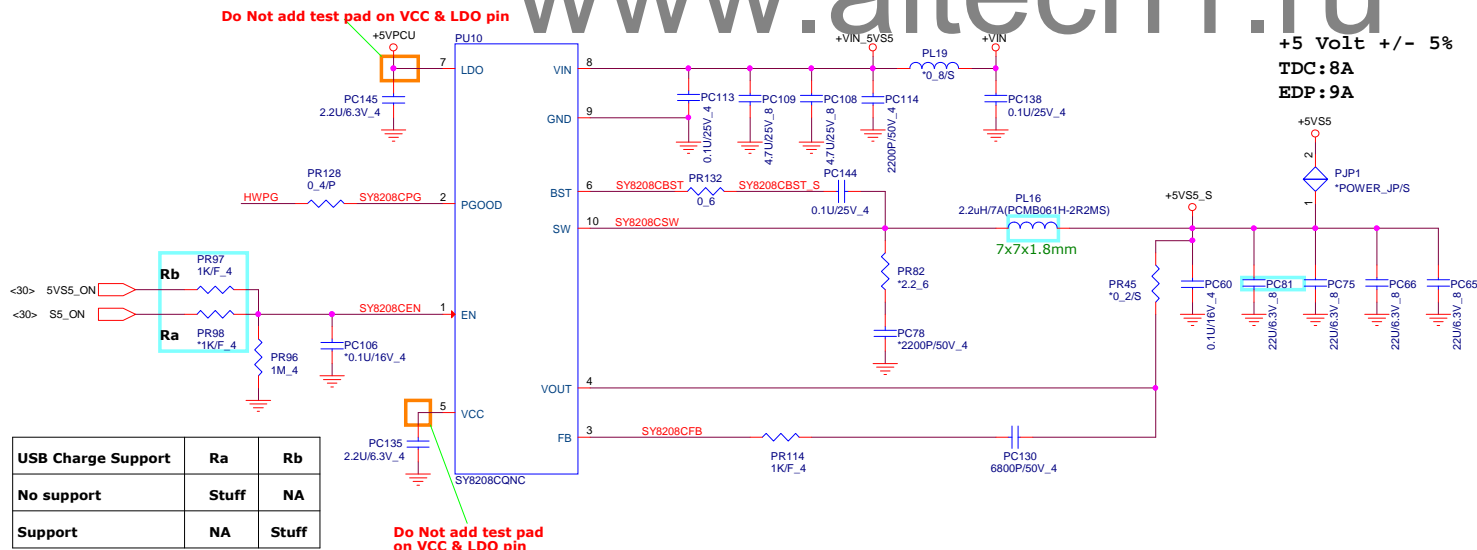




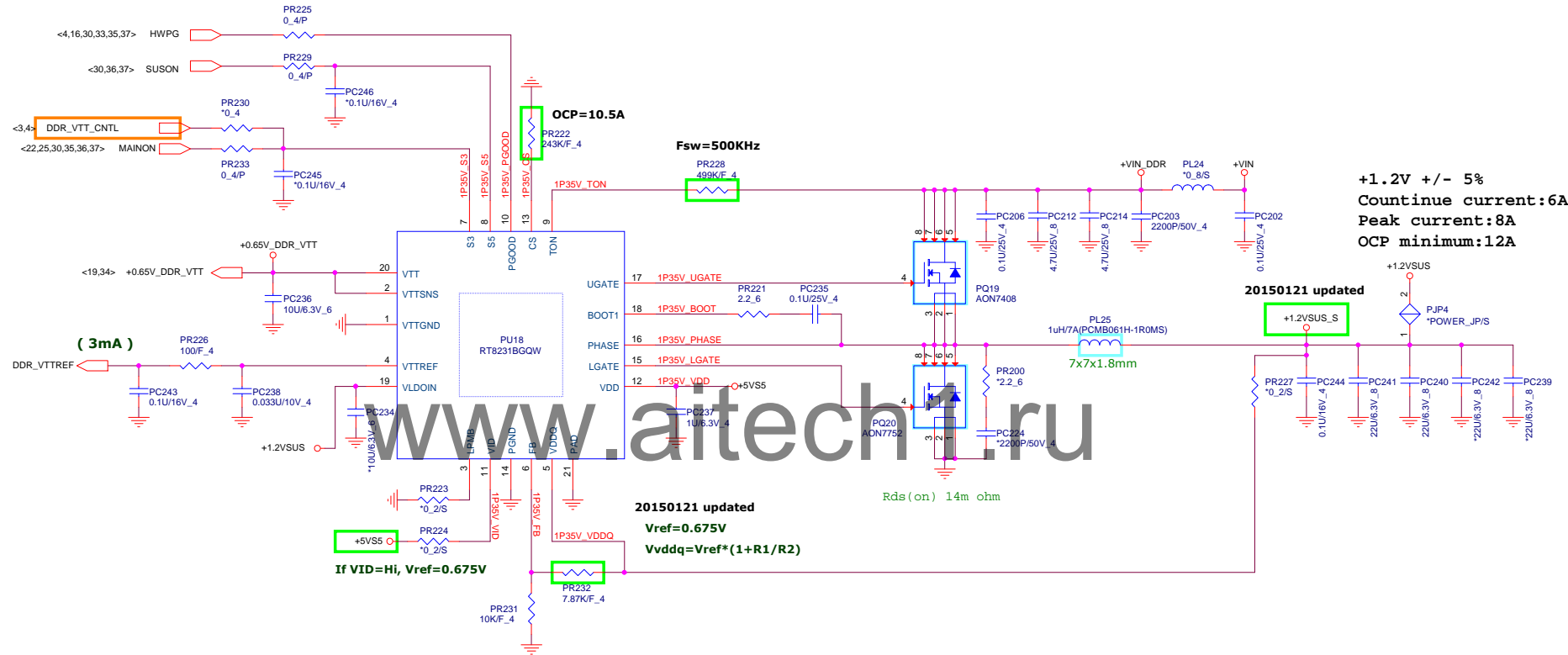




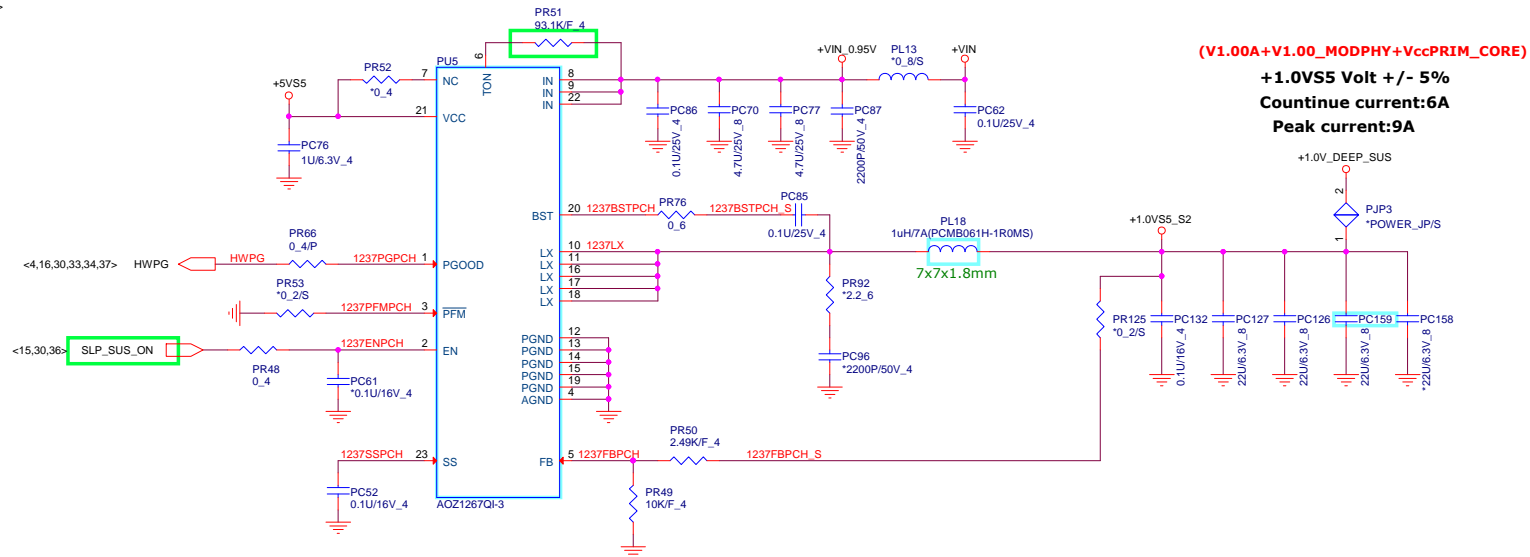
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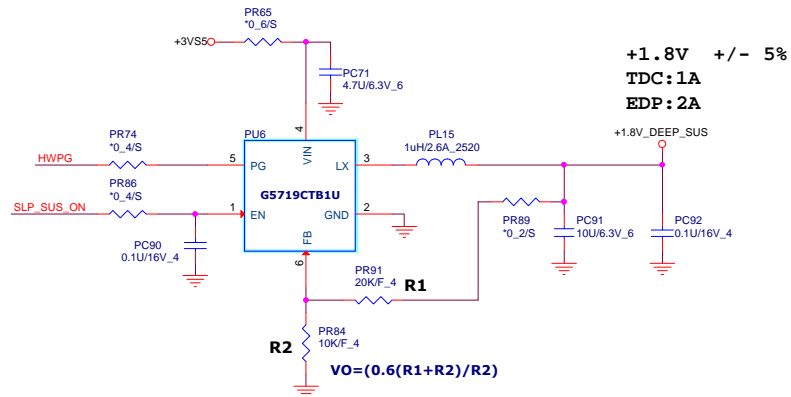
+VIN <15,20,27,30,32,33,35,38,39,40,41>  
 +5VSS <4,25,33,35,36,37>  
 +1.2VSUS <3,6,17,18,36>  
 +0.65V\_DDR\_VTT <19,34>



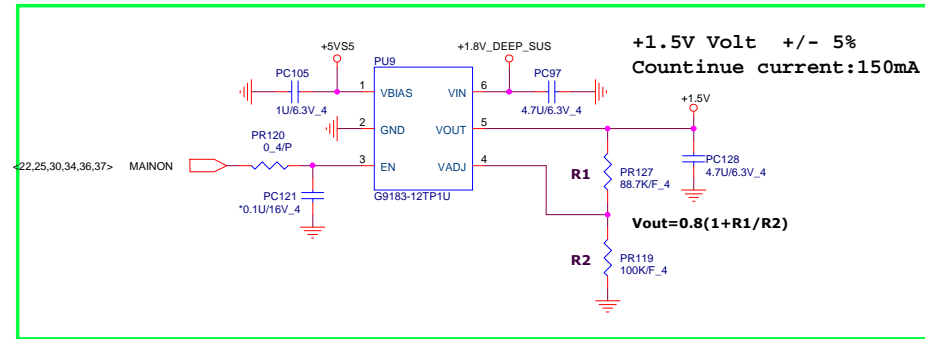
+VIN <15,20,27,30,32,33,34,38,39,40,41>  
 +3VS5 <4,15,16,22,28,30,31,33,36,37>  
 +5VS5 <4,25,33,34,36,37>  
 +1.0V\_DEEP\_SUS <9,13,15,16,36>  
 +1.8V\_DEEP\_SUS <9,15,37>



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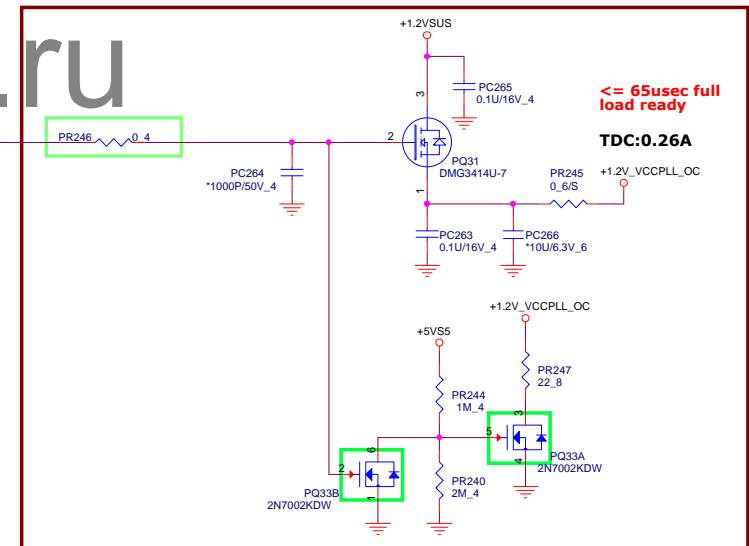
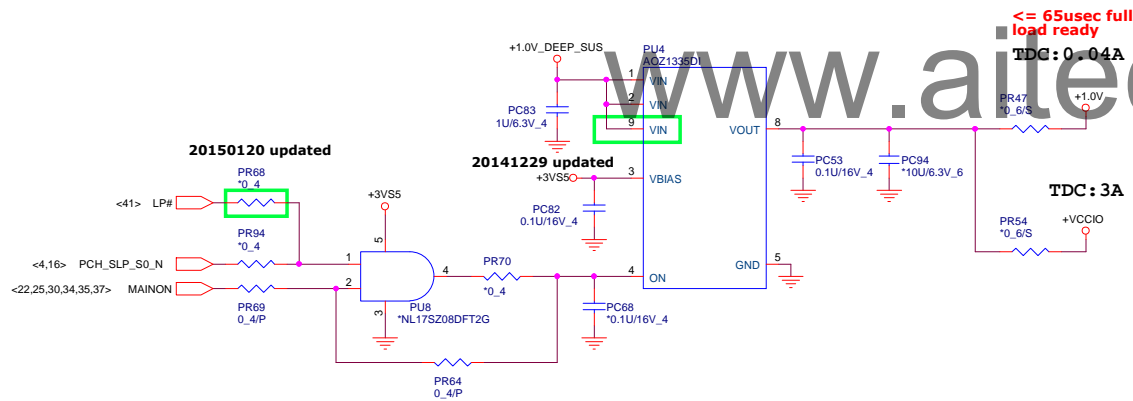
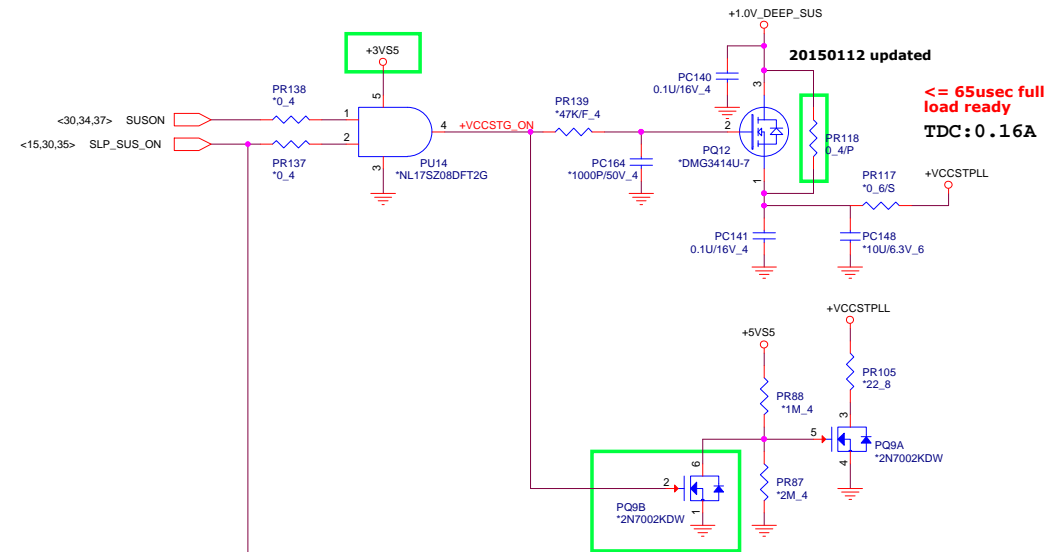
20150116 updated



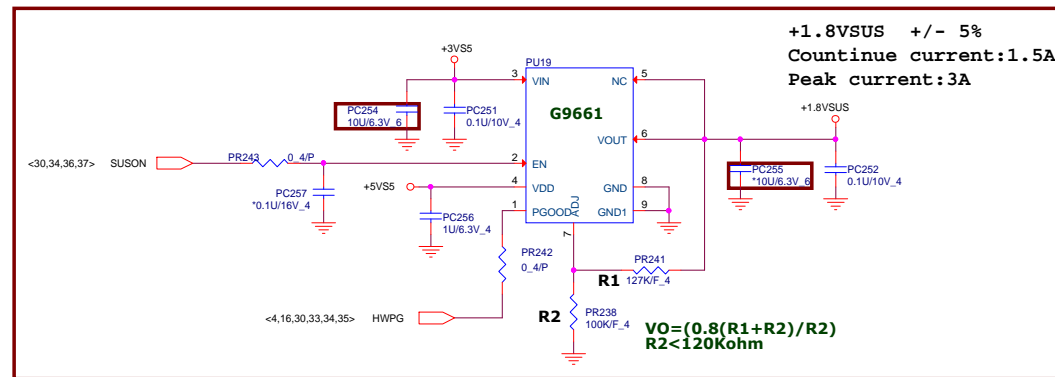
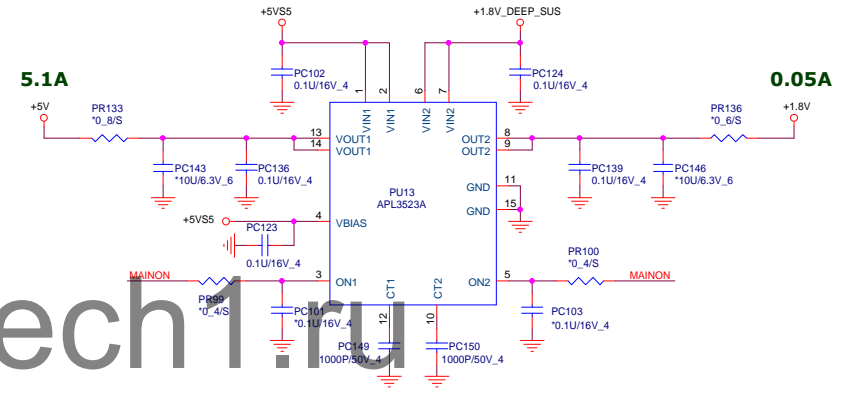
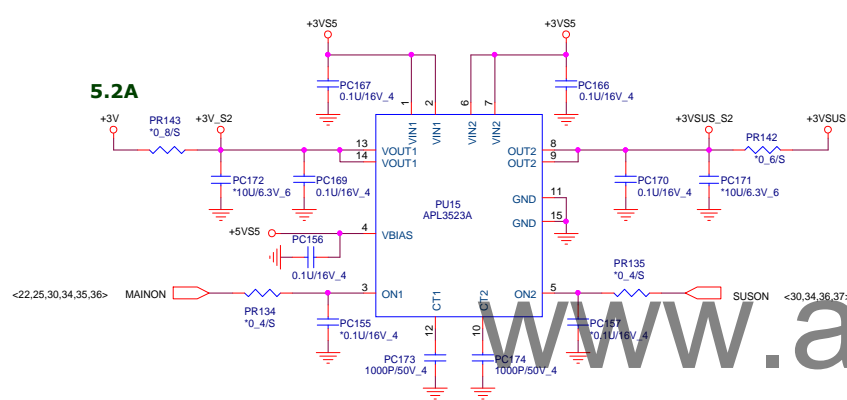
**PROJECT : YODD**  
**Quanta Computer Inc.**

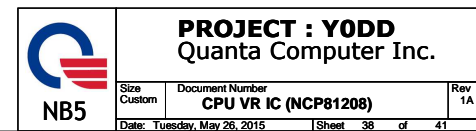
Size Custom	Document Number <b>+1.0/+1.5V/+1.8V_DEEP_SUS</b>	Rev 1A
Date: Tuesday, May 26, 2015	Sheet 35	of 41

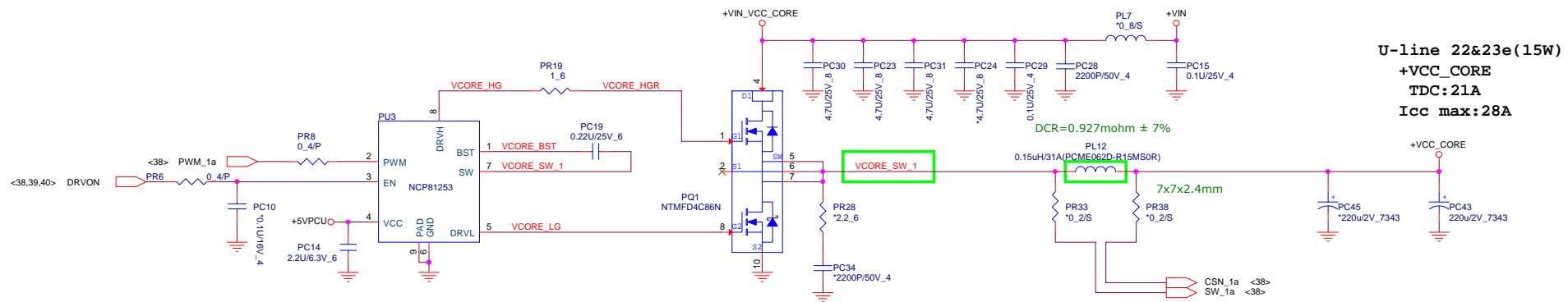
+1.0V <2,4,6,16,30>  
 +3VS5 <4,15,16,22,28,30,31,33,35,37>  
 +5VS5 <4,25,33,34,35,37>  
 +VCCIO <2,6,16>  
 +VCCSTPLL <2,4,5,6,9,38>  
 +1.0V\_DEEP\_SUS <9,13,15,16,35>



+3V <2,4,10,11,12,13,14,15,16,20,21,22,23,25,26,27,29,30,31,38>  
 +5V <22,23,24,27,37,38>  
 +3VS5 <4,15,16,22,28,30,31,33,35,36>  
 +5VS5 <4,25,33,34,35,36>  
 +3VSUS <27,28>  
 +1.8V\_DEEP\_SUS <9,15,35>  
 +1.8V <5,23>  
 +5V <22,23,24,27,37,38>  
 +VIN <15,20,27,30,32,33,34,35,38,39,40,41>  
 +1.8VSUS <17,18>





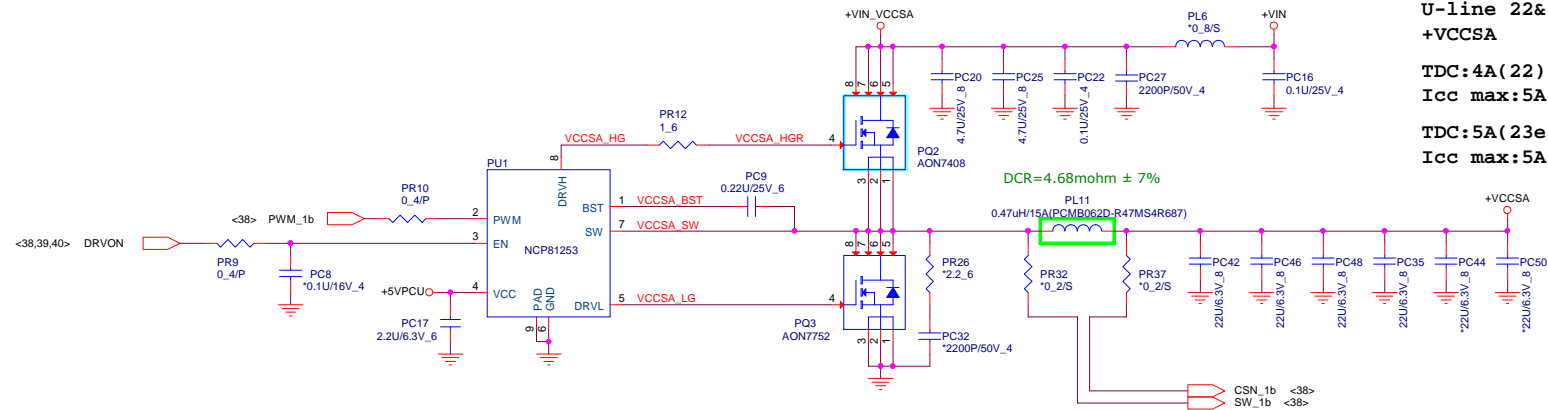


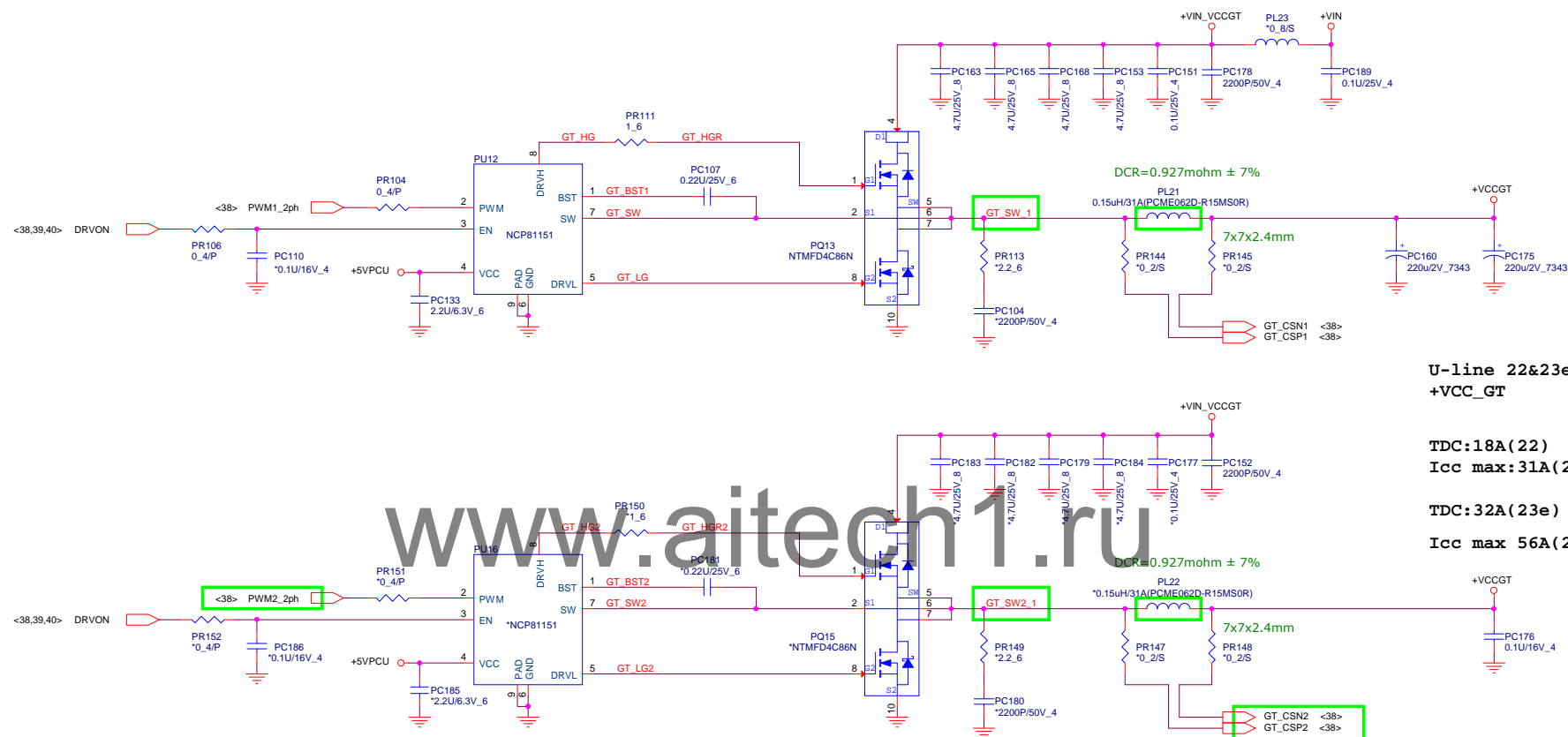
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U-line 22&23e(15W)  
+VCCSA

TDC: 4A(22)  
Icc max: 5A(22)

TDC: 5A(23e)  
Icc max: 5A(23e)

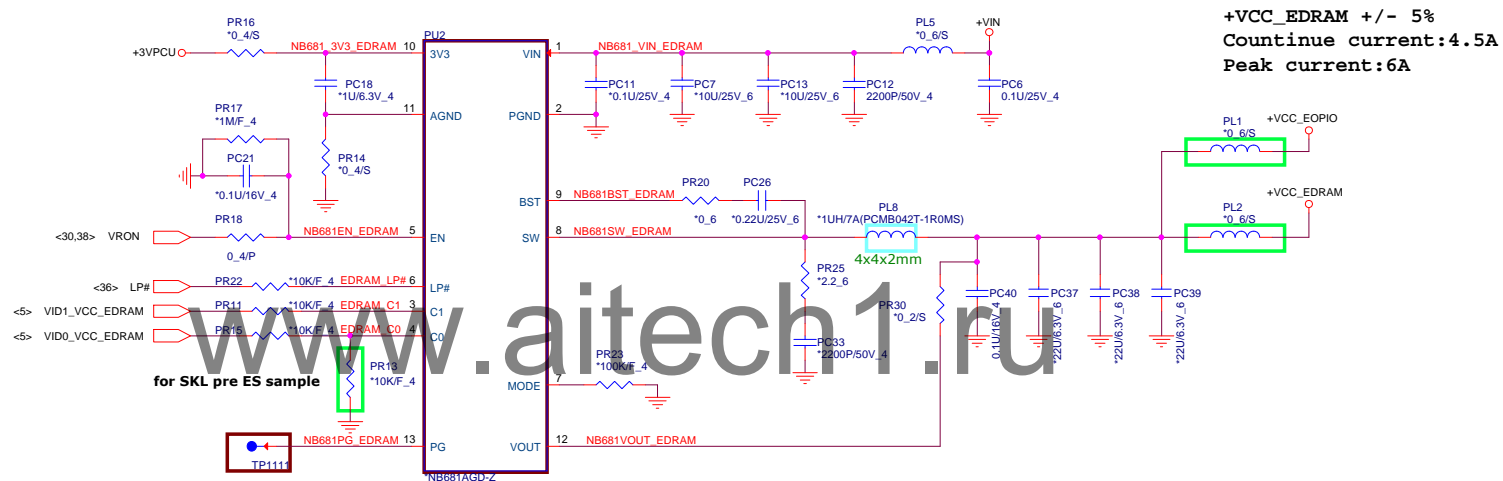
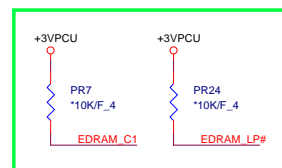




TDC:32A(23e)

Icc max 56A(23e)





VCC\_EDRAM

LP#	C1	C0	Vout
0	X	X	0
1	0	0	0.8
1	0	1	0.95
1	1	0	1.0
1	1	1	1.05

MODE

	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EOPIO	100K
M4	other	150K